



VIGNAN'S INSTITUTE OF MANAGEMENT AND TECHNOLOGY FOR WOMEN

An Autonomous Institution

(Sponsored by Lavu Educational Society)

[Affiliated to JNTUH, Hyderabad & Approved by AICTE, New Delhi]



Department of Electronics and Communication Engineering

BOARD OF STUDIES

S. No	Name of the Member	Designation	Organization	Role
1	Dr. T. Pullaiah	Associate Professor & HOD	VMTW, Hyderabad.	BoS Chairman
2	Dr. T. Satya Savithri	Professor	JNTUH, Hyderabad	Member (JNTUH Nominee)
3	Mr. D. Srinivasa Rao	Project Director	RAILTEL Corporation of India Limited, Secunderabad	Member (Industry)
4	Dr. D. Narendar Singh	Associate Professor	Anurag University, Hyderabad.	Member (Academician)
5	Dr. Vadthiya Narendar	Assistant Professor	NIT, Warangal.	Member (Academician)
6	Ms. A. Sri Lasya	Sr. System Engineer	Cognizant, Hyderabad.	Member (Alumni)
7	Mr. P. Harikrishna	Associate Professor	VMTW, Hyderabad.	Member
8	Dr.SK. Masthan Basha	Associate Professor	VMTW, Hyderabad.	Member
9	Dr. G. Jhansi Reddy	Associate Professor	VMTW, Hyderabad.	Member
10	Dr. K. Padmaleela	Assistant Professor	VMTW, Hyderabad.	Member
11	Mr. J. Sunil Kumar	Associate Professor	VMTW, Hyderabad.	Member
12	Mrs. G. Indira Priyadarshini	Associate Professor	VMTW, Hyderabad.	Member

PRINCIPAL

Principal

Vignan's Institute of Management & Technology For Women
Kondapur (V), Ghatkesar (M), Medchal-Malkajgiri (Dt)-501 301
Telangana State



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Kondapur (V), Ghatkesar (M), Medchal - Malkajgiri (D) - 501 301. Phone: 96529 10002/3



Department of Electronics and Communication Engineering

3rd BoS Meeting on 1st November 2025

AGENDA

Item No.	Agenda Item
1.0	Review and Confirmation of Items
1.1	Review and confirmation of the Minutes of Meeting of the 2nd BoS held on 19 th August 2025.
1.2	Review and Confirmation of M. Tech Academic Regulations (VR25) from the Academic Year: 2025-26.
1.3	Review and Confirmation of M. Tech Academic Calendar (VR25) from the Academic Year: 2025-26.
1.4	Review and Confirmation of M. Tech VLSI System Design Course Structure (VR25) from the Academic Year: 2025-26.
2.0	Approval Items
2.1	Ratification of Syllabus for I M.Tech I Semester.
2.2	Approval of Syllabus for M.Tech II, III & IV Semesters.
3.0	Any other items with permission of Chair


Chairman-BoS



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Department of Electronics and Communication Engineering 3rd BoS Meeting on 1st November 2025

Members Present:

S.No.	Name	Designation	Organization	Position in BoS	Signature
1	Dr.T. Pullaiah	Associate Professor & HOD	VMTW, Hyderabad.	BOS Chairman	
2	Dr.T. Satya Savithri	Professor	JNTUH, Hyderabad	Member (JNTUH Nominee)	
3	Mr. D. Srinivasa Rao	Project Director	RAILTEL Corporation of India Limited, Secunderabad	Member (Industry)	
4	Dr.D. Narendar Singh	Associate Professor	Anurag University, Hyderabad.	Member (Academician)	
5	Dr. Vadthiya Narendar	Assistant Professor	NIT, Warangal.	Member (Academician)	
6	Ms. A. Sri Lasya	Sr. System Engineer	Cognizant, Hyderabad.	Member (Alumni)	
7	Mr. P. Harikrishna	Associate Professor	VMTW, Hyderabad.	Member	
8	Dr.SK.Masthan Basha	Associate Professor	VMTW, Hyderabad.	Member	
9	Dr. G. Jhansi Reddy	Associate Professor	VMTW, Hyderabad.	Member	
10	Dr. K. Padma Leela	Associate Professor	VMTW, Hyderabad.	Member	
11	Mr. J. Sunil Kumar	Associate Professor	VMTW, Hyderabad.	Member	
12	Mrs. G. Indira Priyadarshini	Associate Professor	VMTW, Hyderabad.	Member	

MINUTES BOOK

Vignan's Institute of Management & Technology for Women

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Department of Electronics and Communication Engineering

Minutes of the 3rd Board of Studies (BoS) meeting held on 1st November 2025, 02.00 PM

at Department of ECE, VMTW

The Quorum (minimum 40%) was satisfied.

The Chairman-BoS Dr. T. Pullaiah introduced the following members in the Board.

S. No.	Name	Designation	Organization	Position in BoS
1	Dr. T. Pullaiah	Associate Professor & HOD	VMTW, Hyderabad.	BoS Chairman
2	Dr. T. Satya Savithri	Professor	JNTUH, Hyderabad	Member (JNTUH Nominee)
3	Mr. D. Srinivasa Rao	Project Director	RAILTEL Corporation of India Limited, Secunderabad	Member (Industry)
4	Dr. D. Narendar Singh	Associate Professor	Anurag University, Hyderabad.	Member (Academician)
5	Dr. Vadthiya Narendar	Assistant Professor	NIT, Warangal.	Member (Academician)
6	Ms. A. Sri Lasya	Sr. System Engineer	Cognizant, Hyderabad.	Member (Alumni)
7	Mr. P. Harikrishna	Associate Professor	VMTW, Hyderabad.	Member
8	Dr.SK. Masthan Basha	Associate Professor	VMTW, Hyderabad.	Member
9	Dr. G. Jhansi Reddy	Associate Professor	VMTW, Hyderabad.	Member
10	Dr. K. Padma Leela	Assistant Professor	VMTW, Hyderabad.	Member
11	Mr. J. Sunil Kumar	Associate Professor	VMTW, Hyderabad.	Member
12	Mrs. G. Indira Priyadarshini	Associate Professor	VMTW, Hyderabad.	Member

Minutes of the Board of Studies (BoS) meeting held on Tuesday, 1st November 2025

The following members were present:

1. Dr. T. Pullaiah
2. Dr. T. Satya Savithri
3. Mr. D. Srinivasa Rao
4. Dr. D. Narendar Singh
5. Dr. Vadthiya Narendar
6. Ms. A. Sri Lasya
7. Mr. P. Harikrishna
8. Dr. SK. Masthan Basha
9. Dr. G. Jhansi Reddy
10. Dr. K. Padma Leela
11. Mr. J. Sunil Kumar
12. Mrs. G. Indira Priyadarshini

The Chairman-BoS welcomed all the members to the meeting of the Board of Studies.

Proceedings of the meeting of the Board of Studies

1.0 Review and Confirmation of items

1.1 Review and Confirmation of the Minutes of Meeting of the 2nd BoS held on 19th August 2025.

The Board has reviewed the Minutes of meeting of the 2nd BOS held on 19th August 2025.

1.2 Review and Confirmation of M. Tech Academic Regulations (VR25) from the Academic Year: 2025-26.

The Board has reviewed and confirmed the M. Tech Academic Regulations (VR25) from the Academic Year:2025-26. (Annexure-I).

1.3 Review and Confirmation of M. Tech Academic Calendar (VR25) from the Academic Year: 2025-26.

The Board has reviewed and confirmed the M. Tech Academic Calendar for the A.Y. 2025-26. (Annexure-II).

1.4 Review and Confirmation of M. Tech VLSI System Design Course Structure (VR25) from the Academic Year: 2025-26.

The Board has reviewed and confirmed the M. Tech VLSI System Design Course Structure (VR25) from the Academic year :2025-26. (Annexure-III).

2.0 Approval Items.

2.1 Ratification of Syllabus for I M. Tech I Semester.

The BoS chairman presented the syllabus of I M. Tech VLSI System Design to the members and stated that the syllabus is adopted from JNTUH. (Annexure-IV).

The Board has Approved the Syllabus as per JNTUH.

2.2 Approval of Syllabus for M. Tech II, III & IV Semesters.

The BoS chairman presented the syllabus of M. Tech VLSI System Design II.III & IV semesters to the members and stated that the syllabus is adopted from JNTUH. (Annexure-V).

The Board has Approved the Syllabus as per JNTUH.

3.0 Any other items with permission of Chair

1. Dr. T. Satya Savithri, Professor, JNTUH, Hyderabad observed changes in VR25 with previous syllabus and accepted chosen professional electives.
2. Mr. D. Srinivasa Rao, Project Director, RAILTEL Corporation of India Limited, Secunderabad agreed with Dr. T. Satya Savithri, Professor, JNTUH, Hyderabad
3. Dr. SK. Masthan Basha, Associate Professor, VMTW agreed with Dr. T. Satya Savithri madam,

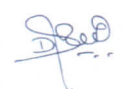
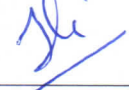
The Board suggested the Chairman_BoS to maintain the Academic Quality, Update the syllabus to uphold the institution's standards.


Chairman - BoS
Dr. T. Pullaiah

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**Minutes of the 3rd Board of Studies (BoS) meeting held on 1st November 2025, 02.00 PM
at Department of ECE, VMTW**

S. No.	Name	Designation	Organization	Position in BoS	Signature
1	Dr. T. Pullaiah	Associate Professor & HOD	VMTW, Hyderabad.	BOS Chairman	
2	Dr. T. Satya Savithri	Professor	JNTUH, Hyderabad	Member (JNTUH Nominee)	
3	Mr. D. Srinivasa Rao	Project Director	RAILTEL Corporation of India Limited, Secunderabad	Member (Industry)	
4	Dr. D. Narendar Singh	Associate Professor	Anurag University, Hyderabad.	Member (Academician)	
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9	Dr. G. Jhansi Reddy	Associate Professor	VMTW, Hyderabad.	Member	
10	Dr. K. Padmaleela	Assistant Professor	VMTW, Hyderabad.	Member	
11	Mr. J. Sunil Kumar	Associate Professor	VMTW, Hyderabad.	Member	
12	Mrs. G. Indira Priyadarshini	Associate Professor	VMTW, Hyderabad.	Member	

Minutes of the Board of Studies (BoS) meeting held on Tuesday, 1st November 2025

ANNEXURE-I



VIGNAN'S INSTITUTE OF MANAGEMENT AND TECHNOLOGY FOR WOMEN

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Academic Regulations (VR25) for M.Tech (Regular) Programme

- 1.0 **Post-Graduate Degree Programmes in Engineering & Technology (PGP in E & T)** Jawaharlal Nehru Technological University Hyderabad (JNTUH) offers **Two** Years (**Four** Semesters) full-time Master of Technology (M. Tech.) Degree programmes, under Choice Based Credit System (CBCS) at its constituent (non-autonomous) and affiliated colleges in different branches of Engineering and Technology with different specializations.
- 2.0 **Eligibility for Admissions**
 - 2.1 Admission to the PGPs shall be made subject to eligibility, qualification and specializations prescribed by the University from time to time, for each specialization under each M. Tech programme.
 - 2.2 Admission to the post graduate programme shall be made on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by Telangana State Government (PGECET) for M. Tech. programmes / an entrance test conducted by JNTUH/ on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.
 - 2.3 The medium of instructions for all PG Programmes will be **ENGLISH** only.
- 3.0 **M. Tech. Programme (PGP in E & T) Structure**
 - 3.1 The M. Tech. Programs in E & T of JNTUH are of Semester pattern, with **Four** Semesters consisting of **Two** academic years, each academic year having **Two** Semesters (First/Odd and Second/Even Semesters). Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per Semester.
 - 3.2 The two-year M. Tech. program consists of **68** credits and the student has to register for all **68** credits and earn all **68** credits for the award of M. Tech. degree. There is **NO** exemption of credits in any case.
 - 3.3 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M. Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M. Tech. programme.
 - 3.4 **UGC/AICTE** specified definitions/descriptions are adopted appropriately for various terms and abbreviations used in these PG academic regulations, as listed below:
 - 3.4.1 **Semester Scheme**

Each Semester shall have 'Continuous Internal Evaluation (CIE)' and 'Semester

End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) are taken as 'references' for the present set of Regulations. The terms 'SUBJECT' and 'COURSE' imply the same meaning here and refer to 'Theory Subject', or 'Lab Course', or 'Design/Drawing Subject', or 'Mini Project with Seminar', or 'Dissertation', as the case may be.

3.4.2 Credit Courses

All subjects/courses are to be registered by the student in a semester to earn credits which shall be assigned to each subject/course in an L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) structure based on the following general pattern:

- One credit for one hour/week/semester for theory/lecture (L) courses
- One credit for two hours/ week/semester for laboratory/ practical (P) courses or tutorials (T)

Other student activities like study tour, guest lecture, conference/workshop participations, technical paper presentations and mandatory courses (*Non-credit Audit Courses*) will not carry any credits.

3.4.3 Subject Course Classification

All subjects/courses offered for the Post-Graduate Programme in E & T (M. Tech. Degree Programme) are broadly classified as follows. The University has followed in general the guidelines issued by AICTE/UGC.

S. No.	Broad Course Classification	Course Group/ Category	Course Description
1	Core Courses (CoC)	PC- Professional Core	Includes subjects related to the parent discipline/department/branch of Engineering
		Dissertation	M. Tech. Project or PG Project or Major Project
		Mini Project with Seminar	Seminar based on core contents related to Parent Discipline/ Department/ Branch of Engineering
2	Elective Courses (EiE)	PE- Professional Electives	Includes elective subjects related to the parent discipline/department/branch of Engineering
		OE-Open Electives	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline/department/ branch of Engineering
3	<i>Mandatory Courses</i>	--	<i>Non-Credit Audit Courses</i>

4.0 Course Registration

- 4.1 A 'Faculty Advisor or Counselor' shall be assigned to each specialization, who will advise on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice/Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

- 4.2 The Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work through 'ON-LINE SUBMISSIONS', ensuring 'DATE and TIME Stamping'. The ON-LINE Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.
- 4.3 A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).
- 4.4 If the Student submits ambiguous choices or multiple options or erroneous entries during ON-LINE Registration for the Subject(s) / Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Subject/ Course in that Category will be taken into consideration.
- 4.5 Subject/ Course Options exercised through ON-LINE Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices also will not be considered. However, if the Subject/ Course that has already been listed for Registration by the University in a Semester could not be offered due to unforeseen or unexpected reasons, then the Student will be allowed to have alternate choice either for a new Subject, if it is offered, or for another existing Subject (subject to availability of seats). Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.
- 5.0 **Attendance Requirements**
The programmes are offered based on a unit system with each subject being considered a unit. Attendance is calculated separately for each subject.
- 5.1 Attendance in all classes (Lectures/Laboratories) is compulsory. The minimum required attendance in each theory subject (*also mandatory Audit Courses*) including the attendance of mid-term examination / Laboratory etc. is 75%. Two periods of attendance for each theory subject shall be considered, if the student appears for the mid-term examination of that subject. *This attendance should also be included in the attendance uploaded every fortnight in the University Website. The attendance of mandatory Audit Courses should be uploaded separately to the University.* A student shall not be permitted to appear for the Semester End Examinations (SEE), if his attendance is less than 75%.
- 5.2 A student's Seminar report and presentation on Mini Project shall be eligible for evaluation, only if he ensures a minimum of 75% of his attendance in Seminar presentation classes on Mini Project during that Semester.
- 5.3 **Condoning of shortage of attendance** (between 65% and 75%) up to a maximum of 10% (considering the days of attendance in sports, games, NCC, NSS activities and Medical grounds) in each subject (Theory/Lab/Mini Project with

Seminar) of a semester shall be granted by the College Academic Committee on genuine reasons.

- 5.4 A prescribed fee per subject shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain relevant documents along with the request from the student.
- 5.5 Shortage of Attendance below 65% in any subject shall in **no case be condoned**.
- 5.6 A Student, whose shortage of attendance is not condoned in any Subject(s) (Theory/Lab/Mini Project with Seminar) in any Semester, is considered as 'Detained in that Subject(s), and is not eligible to write Semester End Examination(s) of such Subject(s), (in case of Mini Project with Seminar, his/her Mini Project with Seminar Report or Presentation are not eligible for evaluation) in that Semester; and he/she has to seek re-registration for those Subject(s) in subsequent Semesters, and attend the same as and when offered.
- 5.7 A student fulfills the attendance requirement in the present semester, shall not be eligible for readmission into the same class.
- 5.8 a) A student shall put in a minimum required attendance in at least **three theory subjects (excluding mandatory (non-credit audit) course)** in first Year I semester for promotion to first Year II Semester.
- b) A student shall put in a minimum required attendance in at least **three theory subjects (excluding mandatory (non-credit audit) course)** in first Year II semester for promotion to second Year I Semester.

6.0 Academic Requirements

The following academic requirements must be satisfied, in addition to the attendance requirements mentioned in item no. 5. The performance of the candidate in each semester shall be evaluated subject- wise, with a maximum of 100 marks per subject / course (theory / practical), based on Internal Evaluation and Semester End Examination.

- 6.1 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course, if he secures not less than:
- 40% of Marks (24 out of 60 marks) in the Semester End Examination;
 - 40% of Marks in the internal examinations (16 out of 40 marks allotted for CIE); and
 - A minimum of 50% of marks in the sum total of CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades this implies securing '**B**' Grade or above in a subject.
- 6.2 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to Mini Project with seminar, if student secures not less than 50% marks (i.e. 50 out of 100 allotted marks). The student would be treated as failed, if student (i) does not submit a seminar report on Mini Project or does not make a presentation of the same before the evaluation committee as per schedule or

(ii) secures less than 50% marks in Mini Project with seminar evaluation. The failed student shall reappear for the above evaluation when the notification for supplementary examination is issued.

- 6.3** A student shall register for all subjects for total of **68** credits as specified and listed in the course structure for the chosen specialization, put in the required attendance and fulfill the academic requirements for securing **68** credits obtaining a minimum of '**B**' Grade or above in each subject, and all **68** credits securing Semester Grade Point Average (**SGPA**) ≥ 6.0 (in each semester) and final Cumulative Grade Point Average (**CGPA**) (i.e., CGPA at the end of PGP) ≥ 6.0 , and shall *pass all the mandatory Audit Courses* to complete the PGP successfully.

Note: (1) The SGPA will be computed and printed on the marks memo only if the candidate passes in all the subjects offered and gets minimum B grade in all the subjects.

(2) CGPA is calculated only when the candidate passes in all the subjects offered in all the semesters

- 6.4** Marks and Letter Grades obtained in all those subjects covering the above specified **68** credits alone shall be considered for the calculation of final CGPA, which will be indicated in the Grade Card /Marks Memo of second year second semester.
- 6.5** If a student registers for extra subject(s) (in the parent department or other departments/ branches of Engineering) other than those listed subjects totaling to **68** credits as specified in the course structure, the performance in extra subject(s) (although evaluated and graded using the same procedure as that of the required **68** credits) will not be considered while calculating the SGPA and CGPA. For such extra subject(s) registered, percentage of marks and Letter Grade alone will be indicated in the Grade Card/Marks Memo, as a performance measure, subject to completion of the attendance and academic requirements as stated in items 5 and 6.1 - 6.3.
- 6.6** When a student is detained due to shortage of attendance in any subject(s) in any semester, no Grade allotment will be made for such subject(s). However, he is eligible for re-registration of such subject(s) in the subsequent semester(s), as and when next offered, with the academic regulations of the batch into which he is re-registered, by paying the prescribed fees per subject. In all these re-registration cases, the student shall have to secure a fresh set of internal marks and Semester End Examination marks for performance evaluation in such subject(s), and SGPA/CGPA calculations.
- 6.7** A student eligible to appear for the Semester End Examination in any subject, but absent from it or failed (failing to secure '**B**' Grade or above), may reappear for that subject at the supplementary examination as and when conducted. In such cases, his Internal Marks assessed earlier for that subject will be carried over, and added to the marks secured in the supplementary examination, for the purpose of evaluating his performance in that subject.

- 6.8** A Student who fails to earn **68** credits as per the specified course structure, and as indicated above, within **four** academic years from the date of commencement of his first year first semester, shall forfeit his seat in M. Tech. programme and his admission **shall stand cancelled**.

7.0 Evaluation - Distribution and Weightage of Marks

The performance of a student in each semester shall be evaluated subject- wise (irrespective of credits assigned) for a maximum of 100 marks.

- 7.1** The performance of a student in every subject/course (including practicals and Project) will be evaluated for 100 marks each, with 40 marks allotted for CIE (Continuous Internal Evaluation) and 60 marks for SEE (Semester End-Examination). The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid-Term Examinations conducted, first Mid-Term examinations in the middle of the Semester and second Mid-Term examinations during the last week of instruction.

- 7.2** In CIE, for theory subjects, during a semester, there shall be two mid-term examinations. Each Mid- Term examination consists of two parts i) **Part – A** for 10 marks, ii) **Part – B** for 20 marks with a total duration of 2 hours as follows:

1. Mid-Term Examination for 30 marks:
 - a. Part - A: Objective/quiz paper for 10 marks.
 - b. Part – B: Descriptive paper for 20 marks.

The objective/quiz paper is set with multiple choice, fill-in the blanks and match the following type of questions for a total of 10 marks. The descriptive paper shall contain 6 full questions out of which, the student has to answer 4 questions, each carrying 5 marks. The average of the two Mid Term Examinations shall be taken as the final marks for Mid Term Examination (for 30 marks).

The remaining 10 marks of Continuous Internal Assessment (out of 40) are distributed as:

2. Assignment for 5 marks. (Average of 2 Assignments each for 5 marks)
3. Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 5 marks.

While the first mid-term examination shall be conducted on 50% of the syllabus, the second mid-term examination shall be conducted on the remaining 50% of the syllabus.

Five (5) marks are allocated for assignments (as specified by the subject teacher concerned). The first assignment should be submitted before the conduct of the first mid-term examination, and the second assignment should be submitted before the conduct of the second mid-term examination. The average of the two assignments shall be taken as the final marks for assignment (for 5 marks).

Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 5 marks before II Mid-Term Examination.

- The Student, in each subject, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and

Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores

$\geq 40\%$ (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

The details of the end semester question paper pattern are as follows:

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equal marks.
- Part-B consists of five questions (numbered from 2 to 6) carrying 10 marks each. Each of these questions is from each unit and may contain sub-questions. For each question there will be an “either” “or” choice, which means that there will be two questions from each unit and the student should answer either of the two questions.
- The duration of Semester End Examination is 3 hours.

7.3 For practical subjects there shall be a Continuous Internal Evaluation (CIE) during the semester for 40 marks and 60 marks for semester end examination. Out of the 40 marks for internal evaluation:

1. A write-up on day-to-day experiment in the laboratory (in terms of aim, components/procedure, expected outcome) which shall be evaluated for 10 marks
2. 10 marks for viva-voce (or) tutorial (or) case study (or) application (or) poster presentation of the course concerned.
3. Internal practical examination conducted by the laboratory teacher concerned shall be evaluated for 10 marks.
4. The remaining 10 marks are for Laboratory Project, which consists of the Design (or) Software / Hardware Model Presentation (or) App Development (or) Prototype Presentation submission which shall be evaluated after completion of laboratory course and before semester end practical examination.

The Semester End Examination shall be conducted with an external examiner and the laboratory teacher. The external examiner shall be appointed from the cluster / other colleges which will be decided by the examination branch of the University.

In the Semester End Examination, held for 3 hours, total 60 marks are divided and allocated as shown below:

1. 10 marks for write-up
 2. 15 for experiment/program
 3. 15 for evaluation of results
 4. 10 marks for presentation on another experiment/program in the same laboratory course and
 5. 10 marks for viva-voce on concerned laboratory course.
- The Student, in each subject, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores

≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

- 7.5 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Principal of the College and this is to be informed to the Director of Evaluation within two weeks, before commencement of the lab end examinations. The external examiner should be selected from outside the College concerned but within the cluster. No external examiner should be appointed from any other College in the same cluster/any other cluster which is run by the same Management.
- 7.6 There shall be Mini Project with Seminar during I year II semester for internal evaluation of 100 marks. The Departmental Academic Committee (DAC) will review the progress of the mini project during the seminar presentations and evaluate the same for 50 marks. Mini Project Viva Voce will be evaluated by the DAC for another 50 marks before the semester end examinations. Student shall carryout the mini project in consultation with the mini project supervisor which may include critically reviewing the literature, project implementation and submit it to the department in the form of a report and shall make an oral presentation before the DAC consisting of Head of the Department, Mini Project supervisor and two other senior faculty members of the department. The student has to secure a minimum of 50% of marks in i) seminar presentation and ii) mini project viva voce, to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same as and when scheduled.
- 7.7 Every candidate shall be required to submit a dissertation on a topic approved by the Dissertation Review Committee.
- 7.8 A Dissertation Review Committee (DRC) shall be constituted with the Head of the Department as Chairperson, Dissertation Supervisor and one senior faculty member of the Department offering the M.Tech. programme.
- 7.9 Registration of Dissertation Work: A candidate is permitted to register for the

Dissertation Work after satisfying the attendance requirement in all the subjects, both theory and laboratory.

- 7.10 After satisfying 7.9, a candidate must present in ***Dissertation Work Review - I***, in consultation with his Dissertation Supervisor, the title, objective and plan of action of his Dissertation work to the Dissertation Review Committee (DRC) for approval ***within four weeks*** from the commencement of **Second year First Semester**. Only after obtaining the approval of the DRC can the student initiate the Dissertation work.
- 7.11 If a candidate wishes to change his supervisor or topic of the Dissertation, he can do so with the approval of the DRC. However, the DRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of Dissertation proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.
- 7.12 A candidate shall submit his Dissertation progress report in two stages at least with a gap of **three** months between them.
- 7.13 The work on the Dissertation shall be initiated at the beginning of the II year and the duration of the Dissertation is two semesters. A candidate is permitted to submit Dissertation Thesis only after successful completion of all theory and practical courses with the approval of DRC ***not earlier than 40 weeks*** from the date of approval of the Dissertation work. For the approval of DRC, the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the DRC.
- 7.14 ***The Dissertation Work Review - II*** in II Year I Semester carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and DRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Dissertation Work. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - II. If he fails to obtain the minimum required marks, he has to reappear for Dissertation Work Review - II as and when conducted.
- 7.15 ***The Dissertation Work Review - III*** in II Year II Sem. carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The DRC will examine the overall progress of the Dissertation Work and decide whether or not the Dissertation is eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Dissertation Work Review - III as and when conducted. For Dissertation Evaluation (Viva Voce) in II Year II Semester there are external marks of 100 and it is evaluated by the external examiner. The candidate has to secure a minimum of 50% marks in Dissertation Evaluation (Viva- Voce) examination.
- 7.16 Dissertation Work Reviews - II and III shall be conducted in phase I (Regular) and Phase II (Supplementary). Phase II will be conducted only for unsuccessful

students in Phase I. The unsuccessful students in Dissertation Work Review - II (Phase II) shall reappear for it at the time of Dissertation Work Review - III (Phase I). These students shall reappear for Dissertation Work Review - III in the next academic year at the time of Dissertation Work Review - II only after completion of Dissertation Work Review - II, and then Dissertation Work Review - III follows. The unsuccessful students in Dissertation Work Review - III (Phase II) shall reappear for Dissertation Work Review - III in the next academic year only at the time of Dissertation Work Review - II (Phase I).

- 7.17 After approval from the DRC, a soft copy of the thesis should be submitted for ANTI-PLAGIARISM check and the plagiarism report should be submitted to the University and be included in the final thesis. The Thesis will be accepted for submission, if the similarity index is less than **30%**. If the similarity index has more than the required percentage, the student is advised to modify accordingly and re-submit the soft copy of the thesis after one month. The maximum number of re-submissions of thesis after plagiarism check is limited to **TWO**. The candidate has to register for the Dissertation work and work for two semesters. After three attempts, the admission is liable to be cancelled. The college authorities are advised to make plagiarism check of every soft copy of theses before submissions.
- 7.18 Three copies of the Dissertation Thesis certified by the supervisor shall be submitted to the College/School/Institute, after submission of a research paper related to the Dissertation work in a UGC approved journal. A copy of the submitted research paper shall be attached to thesis.
- 7.19 The thesis shall be adjudicated by an external examiner selected by the University. For this, the Principal of the College/School/Institute shall submit a panel of **three** examiners from among the list of experts in the relevant specialization as submitted by the supervisor concerned and Head of the Department.
- 7.20 If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unsatisfactory again, the thesis shall be summarily rejected. Subsequent actions for such dissertations may be considered, only on the specific recommendations of the external examiner and /or Dissertation Review Committee. No further correspondence in this matter will be entertained, if there is no specific recommendation for resubmission.
- 7.21 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and decide for the conduct of Dissertation Viva-Voce examination. The Dissertation Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. The candidate has to secure a minimum of 50% of marks in Dissertation Evaluation (Viva-Voce) examination.
- 7.22 If he fails to fulfill the requirements as specified in 7.21, he will reappear for the Dissertation Viva-Voce examination *only after three months*. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for

the award of the degree, unless he is asked to revise and resubmit his Dissertation Work by the board within a specified time period (within *four* years from the date of commencement of his first year first semester).

7.23 The Dissertation Viva-Voce External examination marks must be submitted to the University on the day of the examination.

7.24 *For mandatory non-credit Audit courses, a student has to secure 40 marks out of 100 marks (i.e. 40% of the marks allotted) in the continuous internal evaluation for passing the subject/course. These marks should also be uploaded along with the internal marks of other subjects.*

7.25 *No marks or letter grades shall be allotted for mandatory non-credit Audit Courses. Only Pass/Fail shall be indicated in Grade Card.*

8.0 Re-Admission/Re-Registration

8.1 Re-Admission for Discontinued Student

A student, who has discontinued the M. Tech. degree programme due to any reason whatsoever, may be considered for '**readmission**' into the same degree programme (with the same specialization) with the academic regulations of the batch into which he gets readmitted, with prior permission from the authorities concerned, subject to item 6.6.

8.2 If a student is detained in a subject (s) due to shortage of attendance in any semester, he may be permitted to **re-register** for the same subject(s) in the same category (core or elective group) or equivalent subject, if the same subject is not available, as suggested by the Board of Studies of that department, as and when offered in the subsequent semester(s), with the academic regulations of the batch into which he seeks re-registration, with prior permission from the authorities concerned, subject to item 3.2

8.3 *A candidate shall be given only one-time chance to re-register and attend the classes for a maximum of two subjects in a semester, if the internal marks secured by a candidate are less than 40% and failed in those subjects but fulfilled the attendance requirement. A candidate must re-register for failed subjects within four weeks of commencement of the class work, in the next academic year and secure the required minimum attendance. In the event of the student taking this chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stand cancelled.*

9.0 Examinations and Assessment - The Grading System

9.1 Grades will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Mini Project with Seminar, Dissertation, etc., based on the percentage of marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 7 above, and a corresponding Letter Grade shall be given.

9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured in a subject/Course (Class Intervals)	Letter Grade (UGC Guidelines)	Grade Points
90% and above ($\geq 90\%$, $\leq 100\%$)	O (Outstanding)	10
Below 90% but not less than 80% ($\geq 80\%$, $< 90\%$)	A ⁺ (Excellent)	9
Below 80% but not less than 70% ($\geq 70\%$, $< 80\%$)	A (Very Good)	8
Below 70% but not less than 60% ($\geq 60\%$, $< 70\%$)	B ⁺ (Good)	7
Below 60% but not less than 50% ($\geq 50\%$, $< 60\%$)	B (above Average)	6
Below 50% ($< 50\%$)	F (FAIL)	0
Absent	Ab	0

- 9.3 A student obtaining ‘F’ Grade in any Subject is deemed to have ‘failed’ and is required to reappear as ‘Supplementary Candidate’ for the Semester End Examination (SEE), as and when conducted. In such cases, his Internal Marks (CIE Marks) in those subjects will remain as obtained earlier.
- 9.4 If a student has not appeared for the examinations, ‘Ab’ Grade will be allocated to him for any subject and shall be considered ‘failed’ and will be required to reappear as ‘Supplementary Candidate’ for the Semester End Examination (SEE), as and when conducted.
- 9.5 A Letter Grade does not imply any specific marks percentage; it is only the range of percentage of marks.
- 9.6 In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sake of ‘Grade Improvement’ or ‘SGPA/ CGPA Improvement’.
- 9.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course. The corresponding ‘Credit Points’ (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits For a Course

- 9.8 The student passes the Subject/ Course only when he gets $GP \geq 6$ (B Grade or above).
- 9.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points ($\sum CP$) secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

$$SGPA = \left\{ \sum_{i=1}^N C_i G_i \right\} / \left\{ \sum_{i=1}^N C_i \right\} \dots \text{For each Semester,}$$

where ‘i’ is the Subject indicator index (taking into account all Subjects in a Semester), ‘N’ is the no. of Subjects ‘REGISTERED’ for the Semester (as

specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to the i^{th} Subject, and G_i represents the Grade Points (GP) corresponding to the Letter Grade awarded for that i^{th} Subject.

- 9.10** The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

$$\text{CGPA} = \left\{ \sum_{j=1}^M C_j G_j \right\} / \left\{ \sum_{j=1}^M C_j \right\} \dots \text{for all } S \text{ Semesters registered (ie., up to and inclusive of } S \text{ Semesters, } S \geq 2),$$

where 'M' is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' for from the 1st Semester onwards upto and inclusive of the Semester S (obviously $M > N$), 'j' is the Subject indicator index (taking into account all Subjects from 1 to S Semesters), C_j is the no. of Credits allotted to the j^{th} Subject, and G_j represents the Grade Points (GP) corresponding to the Letter Grade awarded for that j^{th} Subject. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

Illustration of calculation of SGPA

Course/Subject	Credits	Letter Grade	Grade points	Credit Points
Course 1	4	A	8	$4 \times 8 = 32$
Course 2	4	O	10	$4 \times 10 = 40$
Course 3	4	B	6	$4 \times 6 = 24$
Course 4	3	B	6	$3 \times 6 = 18$
Course 5	3	A+	9	$3 \times 9 = 27$
Course 6	3	B	6	$3 \times 6 = 18$
	21			159

$$\text{SGPA} = 159/21 = 7.57$$

Illustration of calculation of CGPA

Semester	Credits	SGPA	Credits * SGPA
Semester I	24	7	$24 \times 7 = 168$
Semester II	24	6	$24 \times 6 = 144$
Semester III	24	6.5	$24 \times 6.5 = 156$
Semester IV	24	6	$24 \times 6 = 144$
	96		612

$$\text{CGPA} = 612/96 = 6.37$$

10.0 Award of Degree and Class

- 10.1** If a student who registers for all the specified Subjects/ Courses as listed in the

Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of **68 Credits** (with CGPA ≥ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with the specialization that he was admitted into.

10.2 Award of Class

After a student has earned the requirements prescribed for the completion of the programme and is eligible for the award of M.Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	$6.75 \leq \text{CGPA} < 7.75$
Second Class	$6.00 \leq \text{CGPA} < 6.75$

A student with final CGPA (at the end of the **PGP**) < 6.00 shall not be eligible for the Award of Degree.

11.0 Withholding of Results

If the student has not paid the dues, if any, to the University or if any case of indiscipline is pending against him, the result and degree of the student will be withheld and he will not be allowed into the next semester.

12.0 General

- 12.1 Credit:** A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.
- 12.2 Credit Point:** It is the product of grade point and number of credits for a course.
- 12.3** Wherever the words "he", "him", "his", occur in the regulations, they shall include "she", "her".
- 12.4** The academic regulation should be read as a whole for the purpose of any interpretation.
- 12.5** In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the University is final.
- 12.6** The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University.

MALPRACTICES RULES**DISCIPLINARY ACTION FOR IMPROPER CONDUCT IN EXAMINATIONS**

S.No	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject to the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination).	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject to the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to

		appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant Superintendent/ any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

	outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s)

		who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
 - (i) A show cause notice shall be issued to the college.
 - (ii) Impose a suitable fine on the college.
 - (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

ANNEXURE-II



VIGNAN'S INSTITUTE OF MANAGEMENT AND TECHNOLOGY FOR WOMEN

(An Autonomous Institution)

[Sponsored by Lavu Educational Society, Affiliated to JNTUH & Approved by AICTE, New Delhi]
Kondapur (V), Ghatkesar (M), Medchal - Malkajgiri (D) - 501 301. Phone: 96529 10002/3



ACADEMIC CALENDAR 2025-26

I- M. Tech I & II SEMESTER

I - SEMESTER

S.No	Event	Date and Day	Duration
1	Commencement of Class Work	13-10-2025(MON)	
2	1 st Spell of Instructions	13-10-2025(MON) to 29-11-2025(SAT)	7 Weeks
3	1 st MID Term Examinations	01-12-2025(MON) to 06-12-2025(SAT)	1 Week
4	2 nd Spell of Instructions	08-12-2025(MON) to 31-01-2026(SAT)	8 Weeks
5	2 nd MID Term Examinations	02-02-2026(MON) to 07-02-2026(SAT)	1 Week
6	Preparation and Practical Examinations	09-02-2026(MON) to 13-02-2026(FRI)	1 Week
7	End Semester Examinations	16-02-2026(MON) to 27-02-2026(FRI)	2 Weeks
8	Commencement of Class Work for II- Semester	02-03-2026(MON)	---

II - SEMESTER

S.No	Event	Date and Day	Duration
1	Commencement of Class Work	02-03-2026(MON)	---
2	1 st Spell of Instructions	02-03-2026(MON) to 18-04-2026(SAT)	7 Weeks
3	1 st MID Term Examinations	20-04-2026(MON) to 24-04-2026(FRI)	1 Week
4	2 nd Spell of Instructions	27-04-2026(MON) to 10-07-2026(FRI)	8 Weeks
5	Summer Vacation	09-05-2026(SAT) to 31-05-2026(SUN)	3 Weeks
6	2 nd MID Term Examinations	13-07-2026(MON) to 18-07-2026(SAT)	1 Week
7	Preparation and Practical Examinations	20-07-2026(MON) to 24-07-2026(FRI)	1 Week
8	End Semester Examinations	27-07-2026(MON) to 07-08-2026(SAT)	2 Week

Principal

Vignani's Institute of Management & Technology For Women
Kondapur (V), Ghatkesar (M), Medchal-Malkajgiri (D)-501301
Telangana State

ANNEXURE-III



VIGNAN'S INSTITUTE OF MANAGEMENT AND TECHNOLOGY FOR WOMEN

(An Autonomous Institution)

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ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI SYSTEM DESIGN

COURSE STRUCTURE – VR25

I M.Tech. – I Semester

S.No.	Course Code	Course	L	T	P	Credits
1	25MV101PC	CMOS Digital IC Design	3	0	0	3
2	25MV102PC	CMOS Analog IC Design	3	0	0	3
3	25MV103PE	1. Device Modeling	3	0	0	3
	25MV104PE	2. Embedded Real Time Operating Systems				
	25MV105PE	3. Nano materials and Nanotechnology				
4	25MV106PE	1. Machine Learning and Deep Learning	3	0	0	3
	25MV107PE	2. VLSI Architectures for Digital Signal Processing				
	25MV108PE	3. Scripting Languages for Design Automation				
5	25MV109PC	CMOS Digital IC Design Laboratory	0	0	4	2
6	25MV110PC	CMOS Analog IC Design Laboratory	0	0	4	2
7	25MV111MS	Research Methodology & IPR	2	0	0	2
8	25MV112AC	Audit Course – I	2	0	0	0
Total			16	0	8	18

I M.Tech. – II Semester

S.No.	Course Code	Course	L	T	P	Credits
1	25MV201PC	Mixed Signal IC Design	3	0	0	3
2	25MV202PC	FPGA Based System Design	3	0	0	3
3	25MV203PE	1. VLSI Test and Testability	3	0	0	3
	25MV204PE	2. Physical Design Automation with AI				
	25MV205PE	3. Functional Verification using System Verilog and UVM				
4	25MV206PE	1. Low Power VLSI Design	3	0	0	3
	25MV207PE	2. Microchip Fabrication Techniques				
	25MV208PE	3. Power Management IC Design				
5	25MV209PC	Mixed Signal IC Design Laboratory	0	0	4	2
6	25MV210PC	FPGA Based System Design Laboratory	0	0	4	2
7	25MV211PC	Mini Project with Seminar	0	0	4	2
8	25MV212AC	Audit Course- II	2	0	0	0
Total			14	0	12	18

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VIGNAN'S INSTITUTE OF MANAGEMENT AND TECHNOLOGY FOR WOMEN

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II M.Tech. – I Semester

S.No.	Course Code	Course	L	T	P	Credits
1	25MV301PC	1. CMOS RF IC Design	3	0	0	3
	25MV302PC	2. Hardware Security in VLSI Design				
	25MV303PC	3. Advanced Memory Design and Architectures				
2	25MV304OE	1. Business Analytics	3	0	0	3
	25MV305OE	2. Industrial Safety				
	25MV306OE	3. Operations Research				
	25MV307OE	4. Cost Management of Engineering Projects	3	0	0	3
	25MV308OE	5. Composite Materials				
3	25MV309PC	Dissertation Work Review – II	0	0	18	6
		Total	6	0	18	12

II M.Tech. – II Semester

S.No.	Course Code	Course	L	T	P	Credits
1	25MV401PC	Dissertation Work Review – III	0	0	18	06
2	25MV402PC	Dissertation Viva-Voce	0	0	42	14
		Total	0	0	60	20

Note: L - Theory T – Tutorial P – Practical

Audit Course I & II:	Open Electives:
- English for Research Paper Writing - Disaster Management - Sanskrit for Technical Knowledge - Value Education - Constitution of India - Pedagogy Studies - Stress Management by yoga - Personality Development Through Life Enlightenment Skills	- Business Analytics - Industrial Safety - Operations Research - Cost Management of Engineering Projects - Composite Materials.

- | | | | |
|----|-----|-----|-----|
| 1. | 2. | 3. | 4. |
| 5. | 6. | 7. | 8. |
| 9. | 10. | 11. | 12. |

ANNEXURE-IV

Vignan's Institute of Management and Technology for Women

An Autonomous Institution

M.Tech.

L T P C

I Year I Semester - VLSI System Design

3 0 0 3

CMOS Digital IC Design

Course Overview

This course introduces students to the foundational and advanced concepts in CMOS (Complementary Metal-Oxide-Semiconductor) digital integrated circuit design. Students will explore the principles, performance metrics, and design strategies for static and dynamic CMOS inverters, combinational and sequential logic gates, and complex digital systems. Emphasis is placed on understanding trade-offs in performance, power, area, and reliability in the context of technology scaling. The course also addresses interconnect modelling and modern layout methodologies, equipping students with practical and theoretical tools for custom and semi-custom digital IC design.

Course Outcomes (COs)

By the end of the course, students will be able to:

- Analyse static and dynamic behaviour of CMOS inverters using key performance metrics.
- Design combinational logic circuits using static and dynamic CMOS styles.
- Implement various sequential logic elements and pipelining techniques.
- Apply custom and semi-custom design methodologies for digital ICs.
- Evaluate interconnect effects and apply techniques to reduce parasitic impact.

Syllabus Unit I:

The CMOS Inverter: Introduction, the static CMOS inverter, Evaluating the robustness of the CMOS inverter – static behavior, Performance of CMOS inverter – dynamic behavior, Power, energy and energy-delay, Technology scaling and its impact on the inverter metrics.

Unit II:

Designing Combinational Logic Gates in CMOS: Introduction, Static CMOS design – complementary CMOS, ratioed logic, pass-transistor logic, Dynamic CMOS design – basic principles, speed and power dissipation of dynamic logic, Issues in dynamic design, cascading dynamic gates, Choosing a logic style, Designing logic for reduced supply voltage.

Unit III:

Designing Sequential Logic Circuits: Introduction – timing metrics for sequential circuits, Classification of memory elements, Static latches and registers – bistability principle, multiplexer-based latches, master-slave edge-triggered register, Low-voltage static latches, static SR flip-flops, Dynamic latches and registers – transmission gate edge-triggered registers, C2MOS, TSPCR, Pipelining – latch vs. register-based pipelines, NORA-CMOS

Unit IV:

Implementation Strategies for Digital ICs: Introduction, From custom to semi-custom and structured array design approaches, Custom circuit design, Cell-based design methodology, Array-based implementation approaches.

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Unit V:

Coping with Interconnect: Introduction, Capacitive parasitics, Resistive parasitics, Inductive parasitics, Advanced interconnect techniques.

Text Book

1. Rabaey, Jan M., Anantha Chandrakasan, and Borivoje Nikolic. *Digital Integrated Circuits: A Design Perspective*. 2nd ed., Pearson Education, 2003.

Reference Books

1. Kang, Sung-Mo (Steve), and Yusuf Leblebici. *CMOS Digital Integrated Circuits: Analysis and Design*. 3rd ed., McGraw-Hill, 2003.
2. Uyemura, John P. *Introduction to VLSI Circuits and Systems*. Wiley, 2002.
3. Weste, Neil H.E., and David Harris. *CMOS VLSI Design: A Circuits and Systems Perspective*. 4th ed., Pearson Education, 2011.

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M.Tech.**L T P C****I Year I Semester - VLSI System Design****3 0 0 3****CMOS Analog IC Design****Course Overview**

This course provides a comprehensive foundation in CMOS Analog Integrated Circuit Design, focusing on the analysis and design of key analog building blocks used in modern VLSI systems. It covers essential topics such as MOS device physics, single-stage and differential amplifiers, current mirrors, and operational amplifiers. Emphasis is placed on understanding the small-signal behavior, frequency response, and performance trade-offs in analog circuits. Students will gain skills in applying transistor-level models, analyzing analog circuit topologies, and designing biasing schemes, enabling them to develop robust analog IC solutions for real-world applications in consumer electronics, communications, and sensor interfaces.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Apply MOS device characteristics and second-order effects to analog circuit analysis.
- Design single-stage MOS amplifier configurations for specific gain and impedance requirements.
- Analyze the performance of differential amplifiers under common-mode and differential-mode operation.
- Apply current mirror topologies to design biasing circuits in CMOS analog design.
- Compare operational amplifier topologies considering gain, bandwidth, and power trade-offs.

Syllabus Unit I:

MOS Device Physics and Models: Introduction to analog design, MOS device physics – General Considerations, MOS I/V Characteristics, Second-Order Effects, MOS Device Models.

Unit II:

Single Stage Amplifiers: Basic Concepts, Common-Source Stage with resistive-load and diode-connected load, Source Follower, Common-Gate Stage.

Unit III:

Differential Amplifiers: Single-Ended and Differential Operation, Basic Differential Pair, Common-Mode Response, Differential Mode with MOS Loads, Gilbert Cell.

Unit-IV

Passive and Active Current Mirrors: Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors

Unit-V:

Operational Amplifiers: General Considerations, One-Stage Op Amps, Two-Stage Op Amps, Gain Boosting, Comparison.

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TextBook

1. Razavi, Behzad. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Education, 2001.

Reference Books

1. Allen, Philip E., and Douglas R. Holberg. *CMOS Analog Circuit Design*. 3rd ed., Oxford University Press, 2011.
2. Johns, David A., and Ken Martin. *Analog Integrated Circuit Design*. Wiley India, 2015.
3. Sansen, Willy M.C. *Analog Design Essentials*. Springer, 2006.

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M.Tech.**L T P C****I Year I Semester - VLSI System Design****3 0 0 3****Device Modeling****Course Overview:**

This course focuses on the theoretical foundations and practical techniques for modeling MOSFET devices in the context of VLSI circuit design. It provides an in-depth understanding of semiconductor device physics, MOS capacitor behavior, MOSFET current-voltage characteristics, and advanced modeling concepts including capacitance, reliability, and parameter extraction. The course also covers how these models are integrated into simulation tools such as SPICE, enabling accurate performance prediction in modern IC design.

Course Outcomes (COs):

By the end of this course, students will be able to:

- Explain the physical structure and electrical behavior of MOSFET devices.
- Analyze and model MOS capacitors and threshold voltage characteristics.
- Develop current-voltage and capacitance models for MOSFETs.
- Evaluate device reliability issues and implement SPICE-based models.
- Apply parameter extraction techniques and statistical modeling in circuit simulation.

Syllabus Unit I:

Fundamentals of MOSFET Structure and Device Physics: Review of semiconductor physics and p-n junction, MOS transistor structure and operation, Scaling effects and parasitics, Modern VLSI device structures

Unit-II:

MOS Capacitor and Threshold Voltage Modeling: MOS capacitor - physics and C-V characteristics, Threshold voltage modeling: uniform and nonuniform doping, Short-channel effects: DIBL, narrow-width effect, Temperature dependence of threshold voltage

Unit-III:

DC and Dynamic Modeling of MOSFETs: Charge-sheet and Pao-Sah current models, Subthreshold conduction and mobility degradation, Temperature effects on current characteristics, Capacitance models: Meyer model, charge-based model, Small-signal modeling

Unit-IV:

Reliability Modeling and SPICE Device Models: Hot-carrier degradation and reliability concerns, Gate and substrate currents, SPICE MOSFET models: LEVEL 1, 2, 3, Parameter definitions and usage in simulation

Unit-V:

Parameter Extraction and Statistical Modeling: Measurement techniques: C-V, threshold voltage, mobility, Parameter extraction using optimization techniques, Statistical modeling for process variation, Worst-case modeling in VLSI design

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Textbook

1. Arora, Narain. *MOSFET Modeling for VLSI Simulation: Theory and Practice*. Springer Science & Business Media, 2007.

Reference Books

1. Tsividis, Yannis, and Colin McAndrew. *Operation and Modeling of the MOS Transistor*. 3rd ed., Oxford University Press, 2011.
 2. Sze, S. M., and Kwok K. Ng. *Physics of Semiconductor Devices*. 3rd ed., Wiley, 2006.
 3. Trivedi, Subarna S., and Saurabh Kumar Gupta. *Semiconductor Device Modeling and Technology*. PHI Learning, 2012.
- Muller, Richard S., and Theodore I. Kamins. *Device Electronics for Integrated Circuits*. 3rd ed., Wil

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I Year I Semester - VLSI System Design	3	0	0	3

Embedded Real Time Operating System

Course Overview

This course provides a comprehensive introduction to Real-Time Operating Systems (RTOS) and their applications in embedded systems. Students will explore the fundamental concepts of real-time embedded systems, understand task management, synchronization mechanisms like semaphores and message queues, and delve into exception handling and timer services. The course also covers memory management strategies and practical techniques for modularizing applications to meet real-time constraints. Additionally, it addresses common design challenges such as deadlocks and priority inversion, preparing students to design, analyse, and implement robust real-time embedded applications.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Analyse key concepts and roles of real-time operating systems in embedded system design.
- Evaluate task scheduling and synchronization methods in real-time systems.
- Design interrupt and timer handling mechanisms for embedded real-time environments.
- Apply real-time memory management techniques in embedded applications.
- Create modular real-time applications to resolve deadlocks and priority inversion.

Syllabus Unit-I:

Introduction to RTOS: Real life examples of embedded systems, real-time embedded systems, the future of embedded systems, a brief history of operating systems, defining an RTOS, the scheduler, objects, services, key characteristics of an RTOS.

Unit-II:

Tasks: Introduction, defining a task, task states and scheduling, typical task operations, typical task structure, synchronization, communication, and concurrency.

Semaphores: Introduction, defining semaphores, typical semaphore operations, typical semaphore use.

Message Queues: Introduction, defining message queues, message queue states, message queue content, message queue storage, typical message queue operations, and typical message queue use.

Unit-III:

Exceptions and Interrupts: Introduction, what are exceptions and interrupts, a closer look at exceptions and interrupts, processing general exceptions, the nature of spurious interrupts.

Timer and Timer Services: Introduction, real-time clocks and system clocks, programmable interval timers, timer interrupt service routines, a model for implementing the soft-timer handling facility, timing wheels, soft timers and timer related operations.

Unit-IV:

Memory Management: Introduction, dynamic memory allocation in embedded systems, fixed-size memory management in embedded systems, blocking vs. non-blocking memory functions, hardware memory management units.

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Unit-V:

Modularizing Applications: Introduction, an outside-in approach to decomposing applications, guidelines and recommendations for identifying concurrency, schedulability analysis – rate monotonic analysis.

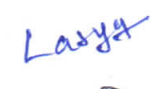
Common Design Problems: Introduction, resource classification, deadlocks, priority inversion.

Text Book

1. Qing Li, and Caroline Yao. *Real-Time Concepts for Embedded Systems*. CMP Books, 2003.

Reference Books

1. Prasad, K. V. K. K. *Embedded Real-Time Systems: Concepts, Design & Programming*. Dream Tech Press, 2005.
2. Simon, David E. *An Embedded Software Primer*. 1st ed., 5th impression, Addison-Wesley Professional, 2007.
3. Singh, Rajib Mall. *Real-Time Systems: Theory and Practice*. Pearson Education India, 2006.

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Nanomaterials and Nanotechnology

Course Overview

This course explores the fundamentals and advanced concepts of nanomaterials and nanotechnologies. It covers the unique physical and chemical properties of nanostructures across different dimensions (0D, 1D, 2D, and 3D), their synthesis methods, and applications. Students will learn about the size-dependent effects on material properties, nanolithography techniques, and the integration of nanomaterials in devices like MEMS and nanoelectronics. Special emphasis is placed on carbon nanotubes (CNTs), ferroelectric materials, and emerging applications in biology, environment, and electronics.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Describe the fundamental properties and classification of nanomaterials across different dimensions.
- Explain the various synthesis methods for nanostructures and their suitability for scaling applications.
- Illustrate the working principles and fabrication processes of MEMS and nanolithography techniques.
- Analyze the growth mechanisms, properties, and applications of carbon nanotubes (CNTs).
- Evaluate the emerging applications of advanced nanomaterials in electronics, biology, and environmental fields.

Syllabus Unit-I:

Introduction to Nanomaterials and Nanotechnologies: Features of nanostructures, Applications of nanomaterials and technologies, Nano-dimensional materials 0D, 1D, 2D structures, Size effects, Fraction of surface atoms, Specific surface energy, Surface stress, Effect on the lattice parameter, Phonon density of states, General methods for synthesis of nanostructures, Precipitative methods, Reactive methods, Hydrothermal/solvothermal methods, Suitability of synthesis methods for scaling, Potential uses.

Unit-II:

Fundamentals and Classification of Nanomaterials: Classification of nanomaterials, Zero- dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nanomaterials, Three-dimensional nanomaterials, Low-dimensional nanomaterials and applications, Synthesis, properties and applications of low-dimensional carbon-related nanomaterials.

Unit-III:

Micro- and Nanolithography Techniques and MEMS: Micro- and nanolithography techniques, Emerging applications, Introduction to MEMS, Advantages and challenges of MEMS, Fabrication technologies, Surface micromachining, Bulk micromachining, Molding, Introduction to nano- photonics.

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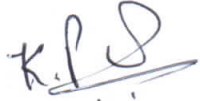
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Unit-IV:

Carbon Nanotubes (CNTs): Introduction to CNTs, Synthesis of CNTs (arc-discharge, laser- ablation, catalytic growth), Growth mechanisms of CNTs, Multi-walled nanotubes, Single-walled nanotubes, Optical properties of CNTs; Electrical transport in perfect nanotubes, Applications of CNTs.

Unit-V:

Advanced Nanomaterials and Applications: Ferroelectric materials, Coating, Molecular electronics, Nanoelectronics, Biological and environmental applications, Membrane-based applications, Polymer-based applications.

Text Book

1. I. Gusev and A. A. Rempel. *Nanocrystalline Materials*. Cambridge International Science Publishing; 1st Indian edition, Viva Books Pvt. Ltd., 2008.
2. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, and James Murday. *Nanoscience and Nanotechnology*. Tata McGraw-Hill Education, 2012.

Reference Books

1. Kenneth J. Klabunde and Ryan M. Richards, editors. *Nanoscale Materials in Chemistry*. 2nd ed., John Wiley & Sons, 2009.
2. Bharat Bhushan. *Springer Handbook of Nanotechnology*. 3rd ed., Springer, 2010.
3. Kamal K. Kar. *Carbon Nanotubes: Synthesis, Characterization and Applications*. 1st ed., Research Publishing Services, 2011.

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I Year I Semester - VLSI System Design	3	0	0	3

Machine Learning and Deep Learning

Course Overview

This course introduces the principles and practices of **Machine Learning and Deep Learning**, focusing on both theoretical understanding and practical implementation. It begins with the fundamentals of machine learning, including learning paradigms, model evaluation, and the challenges that have led to deep learning advances. The course then explores deep neural architectures, including feedforward networks, convolutional and recurrent networks, alongside critical concepts such as regularization and optimization. Finally, students are equipped with practical methodologies for building robust models and exposed to real-world applications across computer vision, speech recognition, and natural language processing.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Analyse machine learning algorithms and evaluate model performance using concepts like overfitting, bias-variance, and likelihood-based estimation.
- Design deep feedforward neural networks using appropriate architectures, activation functions, and backpropagation techniques.
- Apply regularization and optimization techniques to improve generalization and training efficiency of deep neural networks.
- Implement convolutional and recurrent neural network models for processing spatial and sequential data.
- Evaluate model performance and deployment strategies in real-world applications such as computer vision, NLP, and speech recognition.

Syllabus Unit-I:

Machine Learning Basics: Learning algorithms, Capacity, overfitting and underfitting, estimators, bias and variance, maximum likelihood estimation, Bayesian statistics, Supervised and unsupervised learning algorithms, building a machine learning algorithm, challenges motivating deep learning.

Unit-II:

Deep Feedforward Networks: Gradient-based learning, hidden units, architecture design, back-propagation and other differentiation algorithms.

Unit-III:

Regularization for Deep Learning: Norm penalties, Dataset augmentation, multi-task learning, early stopping, sparse representations, ensemble methods, dropout. **Optimization:** Optimization for Training Deep Models, challenges in neural network optimization, basic algorithms, parameter initialization strategies, algorithms with adaptive learning rates.

Unit-IV:

Convolutional Neural Networks: The convolution operation, motivation, pooling, convolution and pooling as an infinitely strong prior, variants of the basic convolution function, structures outputs, data types, efficient convolution algorithms, random or

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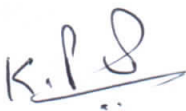
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unsupervised features.

Sequence Modeling:

Recurrent and Recursive Nets, Recurrent Neural Networks, Recursive Neural Networks, Long Short-Term Memory, optimization for long-term dependencies.

Unit-V:

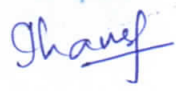
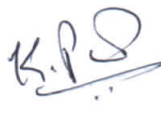
Practical Methodology: Performance metrics, selecting hyperparameters, debugging strategies. **Applications:** Large-scale deep learning, computer vision, speech recognition, natural language processing, other applications.

Text Book

1. Goodfellow, Ian, Yoshua Bengio, and Aaron Courville. *Deep Learning*. MIT Press, 2016.

Reference Books

1. Géron, Aurélien. *Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow*. 2nd ed., O'Reilly Media, 2019.
2. Bishop, Christopher M. *Pattern Recognition and Machine Learning*. Springer, 2006.
3. Chollet, François. *Deep Learning with Python*. 2nd ed., Manning Publications, 2021.

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VLSI Architectures for Digital Signal Processing

Course Overview

This course provides a comprehensive study of Very Large Scale Integration (VLSI) architectures tailored for Digital Signal Processing (DSP) systems. It explores the principles, techniques, and hardware implementations that support high-performance DSP applications in modern CMOS technologies. Topics include algorithmic representations, iteration bounds, pipelining, parallelism, unfolding, folding, and convolution techniques, as well as bit-level and redundant arithmetic architectures. The course also introduces the design and use of programmable DSP processors, with a focus on real-time, low-power, and high-throughput design requirements.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Identify typical DSP algorithms and analyze their computational requirements for efficient VLSI implementation.
- Compute iteration bounds and apply retiming techniques to optimize DSP data flow graphs for performance.
- Design pipelined and parallel FIR filters and utilize unfolding and folding methods for architectural transformations.
- Implement fast convolution methods and develop efficient bit-level and redundant arithmetic units for DSP systems.
- Evaluate and compare programmable DSP processor architectures for various application domains such as mobile and multimedia systems

Syllabus Unit I:

Introduction to Digital Signal Processing Systems: Introduction, typical DSP algorithms, DSP application demands and scaled CMOS technologies. **Iteration Bound:** data-flow graph representations, loop bound, and iteration bound, algorithms for computing iteration bound. **Pipelining and Parallel Processing:** Introduction, pipelining of FIR digital filters, parallel processing. **Retiming:** Definitions and properties, solving systems of inequalities, retiming techniques.

Unit II:

Unfolding: An algorithm for unfolding, properties and applications of unfolding. **Folding:** Folding transformation, register minimization techniques, folding of multirate systems

Unit III:

Fast Convolution: Introduction, Cook-Toom algorithm, Winograd algorithm, iterated convolution, cyclic convolution, design of fast convolution algorithm by inspection.

Unit IV:

Bit-Level Arithmetic Architectures: Introduction, parallel multipliers, bit-serial multipliers, bit-serial filter design and implementation. **Redundant Arithmetic:** Introduction, redundant number representations, carry-free radix-2 addition and subtraction, radix-2 hybrid redundant multiplication architectures, data format conversion, redundancy to nonredundant converter.

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Unit V:

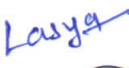
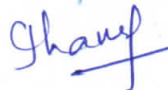
Programmable Digital Signal Processors: Introduction, evolution of programmable digital signal processors, important features of DSP processors, DSP processors for mobile and wireless communications, processors for multimedia signal processing.

Text Book

1. Parhi, Keshab K. *VLSI Digital Signal Processing Systems: Design and Implementation*. Wiley, 1999.

Reference Books

1. V. K. Madisetti, *VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis*, IEEE Press, New York.
2. Meyer-Baese, Uwe. *Digital Signal Processing with Field Programmable Gate Arrays*. 4th ed., Springer, 2014.
3. S. Y. Kung, H. J. Whitehouse, *VLSI and Modern Signal Processing*, Prentice Hall.

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Scripting Languages for Design Automation

Course Overview

This course introduces the use of scripting languages—PERL, TCL, and Python—in the context of Electronic Design Automation (EDA) workflows. Students will learn to write efficient automation scripts for parsing tool outputs, managing design files, and controlling EDA tools such as synthesis and simulation environments. The course emphasizes practical application, covering syntax, control structures, file I/O, regular expressions, and data processing. By the end of the course, learners will be able to automate common VLSI design tasks, improve productivity, and select the appropriate scripting language based on the use case.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Describe the role of scripting languages in EDA workflows and differentiate between scripting and compiled languages.
- Write PERL scripts to perform text parsing, data extraction, and report generation.
- Develop TCL scripts to automate tool commands and control design processes in EDA tools.
- Construct Python scripts for file handling, data processing, and automation of design-related tasks.
- Compare the features of PERL, TCL, and Python, and select suitable scripting languages for specific EDA applications.

Syllabus Unit I:

Introduction to Scripting Languages in EDA: Introduction to scripting and automation, Scripting vs compiled languages, Using interpreters and writing first scripts in Perl, Tcl, and Python, Command-line execution, Variable types and assignments (overview), Control flow basics (if, loops – overview), Basic file I/O (overview), Importance of scripting in EDA tools and flows.

Unit II:

PERL Scripting: Scalar data, Arrays and list data, Hashes, Input and output, Control structures, Regular expressions, Pattern matching with regex, Substitution and translation, Using files and filehandles, String manipulation, Subroutines, Using Perl modules, Command-line arguments and environment variables, Text parsing examples, Report generation

Unit III:

TCL Scripting: Tcl syntax and structure, Variables and data types, Lists and arrays, Expressions and operators, Control flow (if, switch, while, for, foreach), Procedures and variable scope, File input and output, String and list manipulation, Error handling, Working with commands and arguments, Tool-specific scripting conventions, Example tool scripts for synthesis and simulation

Python for Design Automation and Data Processing: Python basics and data types, Expressions and operators, Flow control (if, for, while), Functions, Lists and dictionaries,

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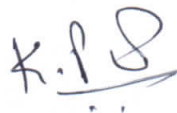
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String manipulation, File reading and writing, Pattern matching with regular expressions, Working with CSV and JSON files, Automating the keyboard and mouse, Using os, sys, and subprocess modules, Writing utility scripts for automation

Unit V:

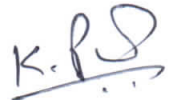
Advanced Integration and Comparison: Comparison of PERL, TCL, and Python features, Strengths and weaknesses in EDA use-cases, Best practices for automation and maintainability, Calling external commands and shell integration in all three languages, Script interoperability using intermediate files (CSV, JSON), Efficiency, readability, and debugging considerations, Choosing the right scripting language for given EDA tasks

Text Books

1. Schwartz, Randal L., brian d foy, and Tom Phoenix. *Learning Perl*. 7th ed., O'Reilly Media, 2016.
2. Welch, Brent B., Ken Jones, and Jeffrey Hobbs. *Practical Programming in Tcl and Tk*. 4th ed., Prentice Hall, 2003.
3. Sweigart, Al. *Automate the Boring Stuff with Python: Practical Programming for Total Beginners*. 2nd ed., No Starch Press, 2019.

Reference Books

1. Robbins, Arnold. *Scripting the UNIX System: Using Bash, Perl, and More*. Addison-Wesley, 2003.
2. Ousterhout, John K. *Tcl and the Tk Toolkit*. 2nd ed., Addison-Wesley Professional, 2009.
3. Python Software Foundation. *Python Language Reference Manual*. <https://docs.python.org>.

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CMOS Digital IC Design Laboratory

Course Overview

This course provides a comprehensive introduction to CMOS digital circuit design, focusing on the fundamental building blocks such as inverters, combinational and sequential logic circuits, and their implementation strategies. Students will explore device physics, design techniques, timing analysis, and the impact of interconnect parasitics on circuit performance. Through practical experiments, learners gain hands-on experience in designing, simulating, and analyzing CMOS circuits, preparing them for advanced work in VLSI and digital IC design.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Design and analyze the static and dynamic behavior of CMOS inverters.
- Implement and simulate basic CMOS combinational logic gates using various design styles.
- Develop and verify sequential logic circuits such as latches and flip-flops.
- Compare different CMOS design methodologies including custom, semi-custom, and array-based approaches.
- Evaluate the impact of interconnect parasitics on the performance and reliability of CMOS circuits.

List of Experiments (Minimum 12 Experiments)

1. **Measure Voltage Transfer Characteristic (VTC) of CMOS Inverter:** Design a static CMOS inverter and plot the input vs. output voltage to determine switching threshold and noise margins.
2. **Determine Propagation Delay of CMOS Inverter:** Apply a square wave input, simulate the output waveform, and measure the rise time, fall time, and propagation delay.
3. **Design and Simulate CMOS NAND Gate:** Implement a 2-input NAND gate using CMOS and verify its truth table and transient response.
4. **Compare Static CMOS and Pass-Transistor NAND Gate:** Design both logic styles for NAND gate, simulate output voltage levels, and compare delay and power.
5. **Design a Dynamic CMOS NOR Gate:** Create a dynamic NOR gate, simulate precharge and evaluation phases, and observe output waveform timing.
6. **Implement and Simulate a Static SR Latch:** Design an SR latch using CMOS transistors; verify bistability by applying input set/reset sequences.
7. **Design a Master-Slave D Flip-Flop:** Build a master-slave edge-triggered flip-flop, apply clock and data inputs, and verify timing and output behavior.
8. **Compare Latch-Based and Register-Based Pipeline Stages:** Design a simple 2-stage pipeline using latches and registers; simulate and compare data propagation delays.

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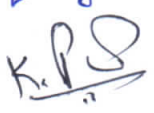
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9. **Custom vs Standard Cell Design of a 2-Input AND Gate:** Implement a 2-input AND gate using full custom transistor-level design and standard cell approach; compare layout area.
10. **Array-Based Implementation of a 2-Bit Adder:** Design a 2-bit adder using an array-based logic style; simulate functional correctness and evaluate area.
11. **Analyze Delay Due to Capacitive Load on CMOS Inverter:** Add different load capacitances to inverter output and simulate the resulting delay variation.
12. **Effect of Interconnect Resistance on Signal Propagation:** Model a resistive interconnect connected to a CMOS inverter output; simulate delay and signal attenuation.
13. **Simulate Interconnect RC Parasitics Impact on Output Waveform:** Extract parasitic RC values for a simple wire segment and simulate their effect on signal rise and fall times.
14. **Compare Signal Integrity with and without Interconnect Inductance:** Model a simple interconnect with inductance; simulate signal ringing and delay effects compared to purely RC models.

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Vignan's Institute of Management and Technology for Women
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M.Tech.**L T P C****I Year I Semester - VLSI System Design****0 0 4 2****CMOS Analog IC Design Laboratory****Course Overview**

This laboratory course complements the theory of analog CMOS design by providing hands-on experience with MOS device characterization, amplifier circuits, differential pairs, current mirrors, and operational amplifiers. Students will learn to design, simulate, and analyze fundamental analog building blocks using industry-standard tools. The experiments emphasize understanding device physics, circuit behavior, and performance trade-offs in real-time conditions, preparing students for practical analog integrated circuit design.

Course Outcomes (COs)

After successful completion of this laboratory course, students will be able to:

- Design and simulate MOS transistors to analyse their electrical characteristics and model parameters.
- Implement and evaluate single-stage amplifiers including common-source, source follower, and common-gate configurations.
- Design differential amplifiers with resistive and active loads and measure their gain and common-mode rejection properties.
- Develop basic, cascode, and active current mirrors, analysing their current replication and output impedance.
- Design and analyse two-stage CMOS operational amplifiers focusing on gain, stability, and frequency response.

List of Experiments (Minimum 12 Experiments)

1. **MOSFET I-V Characteristics Simulation:** Design and simulate NMOS and PMOS transistors to plot I_D vs V_{DS} and I_D vs V_{GS} characteristics; analyze threshold voltage and saturation behavior.
2. **Effect of Second-Order Parameters on MOS Device Performance:** Simulate and study effects like channel length modulation, body effect, and velocity saturation on transistor I-V characteristics.
3. **Extraction of MOS Device Model Parameters Using SPICE:** Extract and verify MOSFET parameters (threshold voltage, mobility, etc.) from device simulation for different model levels.
4. **Design and Simulation of Common-Source Amplifier with Resistive Load:** Design a common-source amplifier and analyze voltage gain, input/output impedance, and frequency response.
5. **Design and Simulation of Common-Source Amplifier with Diode-Connected Load:** Implement a CS amplifier with diode-connected load and compare gain and linearity with resistive-load version.
6. **Design and Analysis of Source Follower (Common-Drain) Amplifier:** Build a source follower circuit; simulate and measure voltage gain, output impedance, and linearity.

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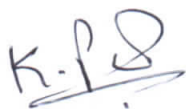
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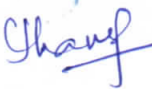
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7. **Design and Simulation of Common-Gate Amplifier:** Design a common-gate stage and analyze its input/output characteristics and high-frequency response.
8. **Design of Basic Differential Pair with Resistive Load:** Simulate a differential pair and analyze differential gain, common-mode gain, and calculate CMRR.
9. **Differential Amplifier with MOS Current Mirror Load:** Implement a differential pair with active current mirror load; analyze improvements in gain and CMRR.
10. **Simulation of Gilbert Cell Mixer:** Design a Gilbert cell circuit and simulate frequency mixing operation with two sinusoidal inputs.
11. **Design and Simulation of Basic Current Mirror:** Implement a basic current mirror; simulate output current accuracy and dependence on transistor sizing.
12. **Design and Simulation of Cascode Current Mirror:** Build a cascode current mirror; analyze output impedance and current matching improvement.
13. **Design of Active Current Mirror Circuits:** Implement Wilson or improved current mirrors; simulate and compare performance with basic and cascode types.
14. **Design and Simulation of Two-Stage CMOS Operational Amplifier:** Design a two-stage op-amp; analyze gain, phase margin, unity gain bandwidth, and frequency response.

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Vignan's Institute of Management and Technology for Women
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M.Tech.	L	T	P	C
I Year I Semester - VLSI System Design	2	0	0	2

Research Methodology and IPR

Course Overview:

This course is designed to introduce students to the fundamental aspects of research methodology and intellectual property rights (IPR). It focuses on identifying and defining research problems, conducting effective literature reviews, writing technical reports and research proposals, and understanding the ethical aspects of research. The course also provides in-depth knowledge of intellectual property laws, including patents, copyrights, trademarks, and geographical indications. Students will learn the process of patenting, the global IPR scenario, and the importance of protecting innovations in a knowledge-driven economy.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Formulate research problems by identifying research gaps, objectives, and scope.
- Analyse literature and research data while ensuring ethical standards and avoiding plagiarism.
- Develop well-structured technical reports and research proposals using appropriate academic formats.
- Evaluate types of intellectual property to determine suitable protection strategies for innovations.
- Apply intellectual property rights concepts to emerging fields such as biotechnology, software, and traditional knowledge.

Syllabus UNIT-I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, Data collection, Analysis, Interpretation, Necessary instrumentations.

UNIT-II:

Effective literature studies approaches, Analysis, Plagiarism, Research ethics.

UNIT-III:

Effective technical writing, how to write a report, paper in developing a research proposal, Format of research proposal, A presentation and assessment by a review committee.

UNIT-IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: Technological research, Innovation, Patenting, Development. International Scenario: International cooperation on Intellectual Property, Procedure for grant of patents, Patenting under PCT.

UNIT-V:

Patent Rights: Scope of Patent Rights, Licensing and transfer of technology, Patent information and databases, Geographical Indications.

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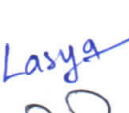
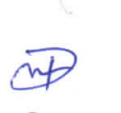
New Developments in IPR: Administration of Patent System, New developments in IPR, IPR of Biological Systems, Computer Software etc. Traditional knowledge, Case Studies, IPR and IITs.

Textbooks:

1. Melville, Stuart, and Wayne Goddard. *Research Methodology: An Introduction for Science & Engineering Students*.
2. Goddard, Wayne, and Stuart Melville. *Research Methodology: An Introduction*.

Reference Books:

1. Kumar, Ranjit. *Research Methodology: A Step-by-Step Guide for Beginners*. 2nd ed.
2. Halbert, Debora J. *Resisting Intellectual Property*. Taylor & Francis, 2007.
3. Mayall, W. H. *Industrial Design*. McGraw-Hill, 1992.
4. Niebel, Benjamin W. *Product Design*. McGraw-Hill, 1974.
5. Asimov, Morris. *Introduction to Design*. Prentice Hall, 1962.
6. Merges, Robert P., Peter S. Menell, and Mark A. Lemley. *Intellectual Property in the New Technological Age*. 2016.
7. Ramappa, T. *Intellectual Property Rights under WTO*. S. Chand, 2008.

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M.Tech. VLSI

L T P C

I Year – I Semester

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ENGLISH FOR RESEARCH PAPER WRITING

Course Objectives: Students will be able to

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first time submission

UNIT - I:

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT - II:

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction.

UNIT - III:

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT - IV:

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

UNIT - V:

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission.

Text Books / Reference :

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM.
Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

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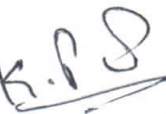
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ANNEXURE-V

Vignan's Institute of Management and Technology for Women
An Autonomous Institution

M.Tech.	L	T	P	C
I Year II Semester - VLSI System Design	3	0	0	3

Mixed Signal IC Design

Course Overview

This course provides a solid foundation in the analysis and design of mixed-signal integrated circuits (ICs), which combine analog and digital functionality on a single chip. It emphasizes signal theory, sampling methods, analog and digital filter design, and the architecture and analysis of data converters. Students will learn the fundamental concepts, mathematical tools, and circuit techniques needed to design real-world mixed-signal systems, with applications in communications, data acquisition, and signal processing.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Analyze sinusoidal signals and frequency-domain representations using Fourier tools and z- transform methods.
- Evaluate the effects of sampling, aliasing, and interpolation on analog signals and implement sample-and-hold circuits.
- Design analog filters using active-RC, MOSFET-C, and gm-C topologies and interpret discrete-time filtering behavior.
- Implement basic digital filters using FIR/IIR techniques and evaluate performance using DAC/ADC SPICE models.
- Assess the performance of data converters based on quantization noise, SNR, and apply noise- shaping methods to improve resolution.

Syllabus Unit I:

Signals, Filters and Tools: Sinusoidal signals, in-phase and quadrature signals, the complex (z-) plane, comb filters – the digital comb filter, the digital differentiator, the digital integrator, representing signals – exponential Fourier series, Fourier transform, Dirac Delta function.

Unit II:

Sampling and Aliasing: Sampling – impulse sampling, decimation, the sample-and-hold (S/H), S/H spectral response, the reconstruction filter (RCF), circuit concerns for implementing the S/H, interpolation, Zero padding, Hold register, linear interpolation, K-path sampling – switched- capacitor circuits, non-overlapping clock generation, implementing the S/H, the S/H with gain.

Unit III:

Analog Filters: Integrator building blocks – low pass filters, active-RC integrators, MOSFET-C integrators, gm-C (transconductance-C) integrators, discrete-time integrators, filtering topologies – the bilinear transfer function, the quadratic transfer function

Unit IV:

Digital Filters – SPICE models for DACs and ADCs, the ideal DAC, the ideal ADC, Sinc-shaped digital filters, band pass and high pass Sinc filters, interpolation using Sinc filters, filtering topologies – FIR filters, the bilinear transfer function, the bilinear transfer function.

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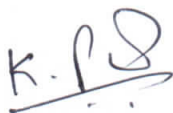
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Unit V:

Data Converters: Quantization noise, signal-to-noise ratio (SNR), clock jitter, improving SNR using averaging, the one-bit ADC and DAC, passive noise-shaping, improving SNR and linearity.

Text Books

1. R. Jacob Baker, *CMOS Mixed-Signal Circuit Design*, Second Edition, Wiley–IEEE Press, 2008.

Reference Books

1. Razavi, Behzad. *Design of Analog CMOS Integrated Circuits*. 2nd ed., McGraw-Hill Education, 2017.
2. Johns, David A., and Ken Martin. *Analog Integrated Circuit Design*. Wiley, 1997.
3. Sansen, Willy M.C. *Analog Design Essentials*. Springer, 2006.
4. Allen, Phillip E., and Douglas R. Holberg. *CMOS Analog Circuit Design*. 2nd ed., Oxford University Press, 2002.

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Vignan's Institute of Management and Technology for Women
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M.Tech.	L	T	P	C
I Year II Semester - VLSI System Design	3	0	0	3
FPGA Based System Design				

Course Overview

This course introduces the principles and practices of FPGA-based system design, with a strong focus on digital logic implementation, system architecture, and modern design methodologies. Students will gain hands-on experience with hardware description languages, combinational and sequential logic design, and explore advanced topics such as platform FPGAs and multi-FPGA systems. The course equips learners with foundational knowledge and practical skills to architect, design, and optimize embedded digital systems using FPGAs. Suitable for postgraduate students in electronics, embedded systems, or VLSI design, this course bridges the gap between traditional digital logic design and modern reconfigurable computing.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Explain the architectural features and functional components of FPGA-based systems and describe their advantages in digital design applications.
- Design combinational logic circuits using Verilog HDL and evaluate them for delay, power, and resource utilization on FPGA platforms.
- Develop and simulate sequential logic circuits and finite state machines using appropriate design styles and clocking rules.
- Apply behavioral design methodologies and demonstrate system modeling using HDLs in real- world case studies.
- Analyze and propose solutions for large-scale FPGA-based systems involving busses, platform FPGAs, and multi-FPGA architectures.

Syllabus UnitI:

Introduction to FPGA-Based Systems: Introduction, basic concepts, digital design and FPGAs, FPGA-based system design, FPGA architectures, SRAM-based FPGAs, permanently programmed FPGAs, chip I/O, circuit design of FPGA fabrics, architecture of FPGA fabrics.

Unit II:

Combinational Logic Design in FPGAs: Introduction, the logic design process, hardware description languages -modeling with HDLs, Verilog, Combinational network delay, power and energy optimization, arithmetic logic, logic implementation for FPGAs, physical design for FPGAs, the logic design process revisited

Unit III:

Sequential Logic and State Machines: Introduction, the sequential machine design process, sequential design styles, rules for clocking, performance analysis, power optimization

Unit IV:

Design Methodologies and Behavioral Architecture: Introduction, behavioral design, design methodologies, design example

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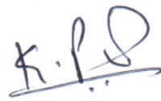
System-Level Design and Advanced FPGA Applications: Introduction, buses, platform FPGAs, multi-FPGA systems, Novel architectures

Text Books

1. Wolf, Wayne. *FPGA-Based System Design*. Pearson Education India, 2005.

Reference Books

1. Maxfield, Clive. *The Design Warrior's Guide to FPGAs: Devices, Tools and Flows*. Newnes, 1st ed., 2004.
2. Trimberger, Stephen M. *Field-Programmable Gate Array Technology*. Springer Science & Business Media, 2012.
3. Kuon, Ian, Russell Tessier, and Jonathan Rose. *FPGA Architecture: Survey and Challenges*. Now Publishers Inc., 2007.

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M.Tech.	L	T	P	C
I Year II Semester - VLSI System Design	3	0	0	3

VLSI Test and Testability

Course Overview

This course introduces students to digital system testing techniques and fault diagnosis in VLSI circuits. It covers fault models, test generation methods for combinational and sequential circuits, and various design-for-testability (DFT) strategies. Students will explore scan-based designs, Built-In Self-Test (BIST) techniques, memory testing algorithms, and fault diagnosis methods. Emphasis is placed on practical testing challenges in digital and embedded systems to ensure reliability and fault tolerance.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Identify different types of faults in digital circuits and explain their corresponding logical fault models.
- Apply test generation techniques to detect faults in combinational and sequential digital circuits.
- Design scan-based and ad-hoc DFT architectures for improving circuit testability.
- Implement Built-In Self-Test (BIST) strategies for digital systems and memory blocks.
- Analyse fault diagnosis techniques to locate and interpret faults in logic-level digital circuits.

Syllabus Unit-I:

Basics of Testing and Fault Modeling: Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.

Unit-II:

Test Generation for Combinational and Sequential Circuits: Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits. Design For Testability

Unit-III:

Design for Testability: Ad-hoc design - Generic scan-based design - Classical scan-based design – System level DFT approaches.

Unit-IV:

Self-Test and Test Algorithms: Built-In Self-Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

Unit-V:

Fault Diagnosis: Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking

Text Books

1. Abramovici, M., M. A. Breuer, and A. D. Friedman. *Digital Systems Testing*

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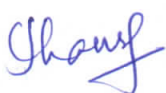
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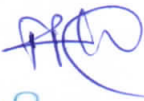
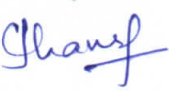
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- and Testable Design*. 1st ed., Jaico Publishing House, 2002.
2. Bushnell, M. L., and V. D. Agrawal. *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. Illustrated ed., Springer Science & Business Media, 2006

Reference Books

1. Lala, P. K. *Digital Circuit Testing and Testability*. Academic Press, 2002.
2. Crouch, A. L. *Design-for-Test for Digital IC's and Embedded Core Systems*. 1st ed., Prentice Hall International, 1999.

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Vignan's Institute of Management and Technology for Women
An Autonomous Institution

M.Tech.	L	T	P	C
I Year II Semester - VLSI System Design	3	0	0	3

Physical Design Automation with AI

Course Overview

This course introduces students to the fundamentals of VLSI physical design and explores how Artificial Intelligence (AI) is transforming Electronic Design Automation (EDA). Students will gain a comprehensive understanding of the VLSI design flow, physical design stages, partitioning algorithms, placement, routing, clock tree synthesis, and timing closure. The course also introduces the role of machine learning in optimizing physical design processes, covering key applications and challenges. Emphasis is placed on design rules, optimization techniques, and algorithmic approaches essential for real-world chip design.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Explain the physical design flow in VLSI and apply basic graph algorithms used in EDA tools.
- Demonstrate understanding of chip planning techniques including floorplanning, placement, and routing.
- Analyze and implement routing strategies and clock tree synthesis for efficient signal distribution.
- Evaluate timing closure techniques to ensure performance and reliability in VLSI designs.
- Identify and discuss the applications and limitations of machine learning in physical design automation.

Syllabus Unit I:

Introduction to Physical Design and AI in EDA: Introduction - Electronic Design Automation (EDA), VLSI Design Flow, VLSI Design Styles, Layout Layers and Design Rules, Physical Design optimizations, Algorithms and Complexity, Graph Theory Terminology, Common EDA Terminology. Netlist and System Partitioning– Introduction, KL and FM Algorithms, Multilevel Partitioning.

Unit-II:

Chip Planning and Placement: Introduction, optimization goals, floorplan representations, floorplanning algorithms, pin assignment, power and ground routing. Global placement, legalization and detailed placement.

Unit-III:

Routing and Clock Tree Synthesis: Introduction, optimization goals, representations of routing regions, the global routing flow, single-net and full-net routing, detailed routing – horizontal and vertical constraint graphs, channel and switchbox routing, area routing, clock routing, modern clock tree synthesis.

Unit – IV:

Timing Closure: Timing analysis, and performance constraints, timing-driven placement, timing- driven routing, physical synthesis, performance-driven design flow.

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Unit-V:

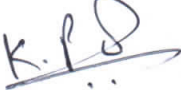
Machine Learning in Physical Design: Introduction ML promises and challenges in physical design, Canonical ML applications, the state of ML for physical design.

Text Book

1. Kahng, Andrew B., et al. *VLSI Physical Design: From Graph Partitioning to Timing Closure*. 2nd ed., Springer International Publishing, 2022.
2. Sherwani, Naveed A. *Algorithms for VLSI Physical Design Automation*. 3rd ed., Springer, 2012.

Reference Books

1. Hsiao, Michael. *Machine Learning Applications in Electronic Design Automation*. Morgan & Claypool, 2020.
2. Cong, Jason, and Bei Yu. *Machine Learning and AI for EDA: From Fundamentals to Advanced Applications*. Springer, 2022.

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Vignan's Institute of Management and Technology for Women
An Autonomous Institution

M.Tech.**L T P C****I Year II Semester - VLSI System Design****3 0 0 3**

Functional Verification using SystemVerilog and UVM

Course Overview

This course provides a comprehensive introduction to functional verification using SystemVerilog and the Universal Verification Methodology (UVM). Starting with foundational SystemVerilog language constructs and object-oriented programming, the course gradually introduces advanced verification concepts including randomization, coverage, and inter-process communication. Building on this foundation, students learn the UVM framework for creating reusable and scalable testbenches, focusing on UVM components, sequences, transactions, and transaction-level modeling (TLM). Hands-on exercises and real-world examples solidify understanding, preparing students for practical verification challenges in ASIC and FPGA design environments.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Write basic SystemVerilog testbenches using data types, control statements, and functions.
- Use object-oriented programming and randomization to create flexible and reusable testbenches.
- Measure verification quality using functional coverage in SystemVerilog.
- Build UVM testbenches using components like tests, drivers, monitors, and agents.
- Use UVM sequences and communication ports to send transactions and collect results.

Syllabus Unit I:

SystemVerilog Fundamentals: Verification Guidelines – Introduction, verification process, basic testbench functionality, testbench components, simulation environment phases, testbench performance. Data Types – built-in data types, arrays, linked lists, creating new types and user-defined structures, constants, strings. Procedural Statements and Routines – tasks, functions, and void functions, routine arguments, returning from a routine. Local data storage, time values.

Unit II:

Testbench and OOP Concepts: Connecting the Testbench and Design—separating the testbench and design, the interface construct, stimulus timing, interface driving and sampling, connecting it all together, program-module interactions, SystemVerilog assertions. Basic OOP – define a class, creating new objects, object deallocation, class routines, dynamic objects, copying objects, building a testbench. Randomization – Introduction, randomization in SystemVerilog, constraint details, solution probabilities, valid and in-line constraints, iterative and array constraints, random control, random generators, random device configuration.

Unit-III:

Advanced Concepts for UVM Readiness: Threads and Interprocess Communication – working with threads, interprocess communication, events, semaphores, mailboxes, building testbench with threads and IPC. Advanced OOP and Testbench Guidelines – inheritance, factory patterns, type casting and virtual methods, composition, inheritance, and alternatives,

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copying an object, callbacks. Functional Coverage – coverage types, strategies, anatomy of a cover group, triggering, data sampling, cross coverage.

Unit-IV:

UVM Infrastructure: Introduction, UVM Components, UVM Tests, UVM Transactions, UVM Sequences

Unit-V:

UVM Integration & TLM (Transaction-Level Modeling) Communication: UVM Agents, Using Analysis Ports in a Testbench, Put and Get Ports in Action, UVM Reporting

Text Book

1. Spear, Chris. *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features*. 2nd ed., Springer, 2014.
2. Salemi, Ray. *UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology*. Mentor Graphics, 2014.

Reference Books

1. Mathur, Ashok B. *Advanced Functional Verification: Concepts and Techniques*. Springer, 2021.
2. Bhasker, J., and Rakesh Chadha. *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features*. Prentice Hall, 2007.
3. Bergeron, Janick. *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features*. 3rd ed., Springer, 2012.

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M.Tech.**L T P C****I Year II Semester - VLSI System Design****3 0 0 3****Low Power VLSI Design****Course Overview**

This course focuses on the principles and techniques for designing energy-efficient CMOS VLSI circuits. Students will learn about the sources and modeling of power dissipation in modern integrated circuits, and methods for estimating and optimizing power consumption at various design levels. Topics include low-power design strategies at the device, circuit, logic, architecture, and software levels. The course also explores emerging techniques like adiabatic computing, pass-transistor logic, and asynchronous circuit design for ultra-low-power applications.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Identify sources of power dissipation in CMOS circuits and explain methods to reduce them.
- Apply power estimation techniques to evaluate energy usage in combinational and sequential logic circuits.
- Use architectural and circuit-level transformations to optimize designs for low power consumption.
- Design and test low-voltage CMOS circuits considering submicron effects and leakage currents.
- Explore and apply advanced low-power techniques such as adiabatic logic and software-level power optimization.

Syllabus Unit I:

Low-Power CMOS VLSI Design: Introduction, Sources of Power Dissipation, Designing for Low Power. Physics of Power Dissipation in CMOS FET Devices- MIS structure, Long Channel and Sub-micron MOSFET, Gate Induced Drain Leakage, Power dissipation in CMOS-Short Circuit and Dynamic Dissipation, Load Capacitance.

Unit II:

Power Estimation in CMOS Circuits: Modelling of signals, Signal Probability Calculation, Probabilistic Techniques for Signal Activity Estimation. Statistical Techniques -Estimating Average Power in Combinational and Sequential Circuits, Estimation of Glitching Power, Power Estimation using Input Vector Compaction, Power Dissipation in Domino CMOS.

Unit III:

Synthesis for Low Power: Behavioural Level Transforms - Algorithm Level Transforms, Power Constrained Least Squares Optimization for Adaptive and Non-adaptive Filters, Circuit Activity Driven Architectural Transformations, Architecture Driven Voltage Scaling, Power Optimization using Operation Reduction and Substitution, Precomputation-Based Optimization for Low Power, Logic and Circuit Level Optimization for Low Power.

Unit IV:

Design and Test of Low Voltage CMOS Circuits: Introduction, Circuit Design Styles, Leakage Current in Deep Sub-micrometer Transistors, Deep Sub-micrometer Device

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Design Issues, Minimizing Short Channel Effect, Low Voltage Circuit Design Techniques – Reverse Vgs, Steeper Subthreshold Swing, Multiple Threshold Voltages, Multiple Supply Voltages.

Unit V:

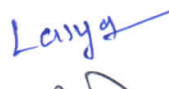
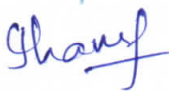
Advanced Techniques: Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits. Software Design for Low Power: Introduction, Sources of Software Power Dissipation, Software Power Estimation and Optimization.

Text Book

1. Roy, Kaushik, and Sharat C. Prasad. *Low-Power CMOS VLSI Circuit Design*. Wiley-IEEE Press, 2000.
2. Rabaey, Jan M., Anantha Chandrakasan, and Borivoje Nikolic. *Digital Integrated Circuits: A Design Perspective*. 2nd ed., Prentice Hall, 2003.

Reference Books

1. Chandrakasan, Anantha P., and Robert W. Brodersen. *Low Power Digital CMOS Design*. Kluwer Academic Publishers, 1995.
2. Pedram, Massoud. *Power-Aware Design Methodologies*. Springer, 2005.

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Vignan's Institute of Management and Technology for Women
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M.Tech.**L T P C****I Year II Semester - VLSI System Design****3 0 0 3**

Microchip Fabrication Techniques

Course Overview

This course provides a comprehensive introduction to the principles and processes involved in semiconductor fabrication, focusing on silicon-based microchip manufacturing. Students will explore the semiconductor industry, material properties, and crystal growth techniques essential for wafer preparation. The course covers wafer fabrication methods, contamination control, and yield optimization. Key lithography and patterning techniques, including advanced photolithography, doping, and thin-film deposition, are studied in detail. Finally, metallization, device evaluation, packaging, and the business aspects of wafer fabrication complete the curriculum, preparing students for roles in VLSI fabrication and semiconductor manufacturing industries.

Course Outcomes:

By the end of this course, students will be able to:

- Describe the semiconductor industry landscape and explain the properties of semiconductor materials and wafer preparation techniques.
- Outline the wafer fabrication process and apply contamination control and productivity improvement methods.
- Demonstrate understanding of lithography and patterning processes used in semiconductor manufacturing.
- Explain advanced lithography techniques, doping processes, and thin-film deposition methods for device fabrication.
- Analyze metallization techniques, device evaluation procedures, packaging methods, and the business considerations of wafer fabrication.

Syllabus Unit-I:

Semiconductor Industry and Materials: The Semiconductor Industry, Properties of Semiconductor Materials and Chemicals, Crystal Growth and Silicon Wafer Preparation

Unit-II:

Wafer Fabrication and Contamination Control: Overview of Wafer Fabrication, Contamination Control, Productivity and Process Yields, Oxidation

Unit-III:

Lithography Processes – Patterning Steps: The Ten-Step Patterning Process — Surface Preparation to Exposure, The Ten-Step Patterning Process — Developing to Final Inspection

Unit-IV:

Advanced Lithography, Doping, and Deposition: Advanced Photolithography Processes, Doping, Layer Deposition

Unit-V:

Metallization, Device Evaluation, Business, and Packaging: Metallization, Process and Device Evaluation, The Business of Wafer Fabrication, Introduction to Devices and Integrated Circuit Formation, Introduction to Integrated Circuits, Packaging

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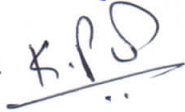
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1. Van Zant, Peter. *Microchip Fabrication: A Practical Guide to Semiconductor Processing*. 6th ed., McGraw-Hill, 2014.

Reference Books

1. Ghandhi, Sorab K. *VLSI Fabrication Principles: Silicon and Gallium Arsenide*. 2nd ed., Wiley, 1994.
2. Sze, Simon M., and Kwok K. Ng. *Physics of Semiconductor Devices*. 3rd ed., Wiley- Interscience, 2006.
3. Streetman, Ben G., and Sanjay Banerjee. *Solid State Electronic Devices*. 7th ed., Pearson, 2014.
4. Wolf, Stephen, and Richard N. Tauber. *Silicon Processing for the VLSI Era*. Vol. 1, Lattice Press, 1986.

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M.Tech.**L T P C****I Year II Semester - VLSI System Design****3 0 0 3**

Power Management IC Design

Course Overview

This course provides a comprehensive understanding of modern Power Management Integrated Circuits (PMICs), emphasizing the principles, design methodologies, and implementation challenges across various topologies such as linear regulators, inductive converters, and switched-capacitor converters. Through theoretical analysis and practical case studies (e.g., smartphones and IoT), students will develop skills to design energy-efficient, high-performance power management solutions suited for SoCs and complex embedded systems. The course also includes peripheral circuit design for sensing, protection, and control integration.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Describe the roles, architectures, and functional requirements of Power Management ICs (PMICs) and their application in modern electronic systems.
- Design linear voltage regulators, including advanced and digital LDOs, considering efficiency, stability, and transient performance.
- Analyse inductive DC-DC converter topologies (buck, boost, buck-boost, multi-phase, SIMO) with emphasis on performance metrics and control techniques.
- Implement switched capacitor and charge pump converters for integrated, compact, and efficient power management solutions.
- Integrate gate driver circuits, protection mechanisms, and sensing modules to ensure reliability and safety in PMICs.

Syllabus Unit-I:

Fundamentals of Power Management ICs: Role and requirements of Power Management ICs (PMICs), the smartphone as a typical example, fundamental concepts - linear regulator, the inductive DC-DC converter, the Switched capacitor converters, the hybrid converter, power delivery - lateral and vertical, integrated voltage regulator (IVR), dynamic voltage and frequency scaling (DVFS).

Unit-II:

Linear Voltage Regulators: Fundamental circuit and control concept, drop voltage and power efficiency, frequency behavior and stability, fast transient techniques and slew-rate enhancement, PSRR, output noise, soft-start, Advanced LDO types: capacitor-less, flipped voltage follower, Digital LDOs: ADC, digital controller, limit cycle oscillations.

Unit-III:

Inductive DC-DC Converters: The fundamental Buck converter, voltage conversion ratio, ripple, losses and power conversion efficiency, inductor and capacitor sizing, voltage-mode and current-mode control, Loop compensation: Type I, II, III compensators, Constant on-time and hysteretic control, DCM operation and burst mode, Boost, buck-boost, and flyback converters, Multi-phase converters: ripple cancellation, phase shedding, Single inductor multiple output (SIMO) converters.

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Unit-IV:

Switched-Capacitor (SC) and Charge Pump Converters: Basic operation of charge pumps: diode-based and transistor-based, Parasitic effects, charge sharing, and efficiency, SC converter topologies: Dickson, ladder, Fibonacci, Charge flow modeling and output resistance, Gate drive techniques, Capacitor and switch sizing, multi-phase and multi-ratio SC converters, interleaving, ripple reduction, and closed-loop control.

Unit-V:

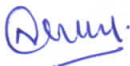
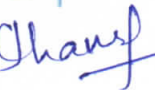
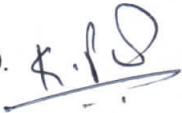
Gate Drivers, Protection, and Sensing: Gate driver architectures: CMOS inverters, cascaded drivers, Bootstrap techniques and dv/dt triggering, Level shifters: resistor-based, cross-coupled, capacitive, Current sensing methods: shunt, replica, DCR, Protection circuits: OVP, thermal shutdown, UVLO, power-on-reset, Bandgap reference circuits and trimming, Zero-cross detection and current limiting.

Text Books

1. Wicht, Bernhard. *Design of Power Management Integrated Circuits*. Wiley, 2024.

Reference Books

1. Erickson, Robert W., and Dragan Maksimovic. *Fundamentals of Power Electronics*. 2nd ed., Springer, 2001.
2. Basso, Christophe. *Switch-Mode Power Supplies: SPICE Simulations and Practical Designs*. McGraw-Hill Education, 2008.
3. Wu, Jinrong, and Ray Ridley. *Power Supply Design: A Practical Guide*. Springer, 2019.

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M.Tech.**L T P C****I Year II Semester - VLSI System Design****0 0 4 2**

Mixed Signal IC Design Laboratory

Course Overview

This course introduces the fundamental concepts of signal processing and filter design, focusing on both analog and digital domains. Students will explore signal representation, sampling theory, aliasing, and various filtering techniques including analog integrators, digital filters, and data converters. The course combines theoretical knowledge with practical experiments to develop skills in designing, simulating, and analyzing signal processing circuits and systems.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Analyze and represent signals using sinusoidal components and the complex z-plane.
- Design and evaluate sample-and-hold circuits and interpolation techniques to mitigate aliasing effects.
- Implement and analyze analog filter circuits including active-RC, MOSFET-C, and gm-C integrators.
- Design and simulate digital filters such as comb, Sinc-shaped, and FIR filters using bilinear transform methods.
- Model and evaluate the performance of data converters including ideal DACs and ADCs.

List of Experiments (Minimum 12 Experiments)

1. **Sinusoidal Signals and Quadrature Components:** Generate and analyze sinusoidal signals including their in-phase and quadrature components to understand signal representation.
2. **Signal Representation on Complex (z-) Plane:** Plot signals on the complex z-plane and analyze their magnitude and phase characteristics.
3. **Digital Comb Filter Design:** Design and simulate a digital comb filter and analyze its frequency response to understand notch filtering.
4. **Digital Differentiator and Integrator:** Implement digital differentiator and integrator circuits and analyze their time and frequency domain responses.
5. **Impulse Sampling and Aliasing Analysis:** Simulate impulse sampling and study the aliasing effect in the frequency spectrum of the sampled signal.
6. **Sample-and-Hold (S/H) Circuit Analysis:** Design a sample-and-hold circuit and analyze its spectral response and effect on signal reconstruction.
7. **Interpolation Techniques:** Implement zero padding and linear interpolation methods on sampled data to improve signal resolution.
8. **Switched-Capacitor Sample-and-Hold Circuit:** Design a switched-capacitor sample-and-hold circuit with non-overlapping clocks and analyze its performance.
9. **Active-RC Low-Pass Integrator Design:** Design and simulate an active-RC low-pass integrator filter and analyze its frequency response.

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10. **MOSFET-C and gm-C Integrator Design:** Implement MOSFET-C and gm-C integrators, compare their characteristics and frequency response.
11. **Discrete-Time Integrator Design:** Design and analyze discrete-time integrator circuits to understand their filtering behavior. **Ideal DAC and ADC Modeling:** Model ideal DAC and ADC circuits, and analyze their input- output characteristics and linearity.
12. **Sinc-Shaped Digital Filter Design:** Design Sinc-shaped digital filters including bandpass and highpass filters and analyze their frequency response.
13. **FIR Filter Implementation Using Bilinear Transfer Function:** Implement FIR filters using the bilinear transfer function and analyze filter characteristics like gain and phase response.

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M.Tech.	L	T	P	C
I Year II Semester - VLSI System Design	0	0	4	2

FPGA Based System Design Laboratory

Course Overview

This laboratory course focuses on practical hands-on experience with FPGA design and implementation using Hardware Description Languages (HDLs) such as Verilog or VHDL. Students will learn to design, simulate, and implement fundamental digital building blocks, combinational and sequential circuits, and complex systems like finite state machines and communication modules on FPGA platforms. The course covers a range of topics from basic logic gates and arithmetic units to real-time systems and digital signal processing applications. Emphasis is placed on simulation, verification, and hardware validation to bridge the gap between theoretical concepts and real-world digital system design.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Write and simulate HDL code for basic combinational and sequential digital circuits using Verilog HDL.
- Design and implement complex digital systems such as FSMs, arithmetic logic units, and communication modules on FPGA platforms.
- Develop and verify interfacing protocols for external hardware devices like seven-segment displays, keypads, and UART communication.
- Apply design methodologies for timing, synchronization, and resource optimization in FPGA-based digital system design.
- Demonstrate the ability to deploy and debug digital designs on FPGA development boards, validating functionality through hardware testing

List of Experiments (Any 12 Experiments)

1. **LED Blinking Using Verilog:** Implement a basic LED blink circuit to understand FPGA programming and output pin control.
2. **Design and Simulation of Basic Logic Gates using Verilog HDL:** To write HDL code for basic logic gates (AND, OR, NOT, XOR), simulate their functionality, and verify the outputs using a waveform viewer.
3. **Implementation of 4-bit Adder/Subtractor on FPGA:** To design and implement a 4-bit adder/subtractor using Verilog, simulate and verify functionality on an FPGA development board.
4. **Design of a 4x1 Multiplexer and 1x4 Demultiplexer:** To write and simulate Verilog code for a 4x1 MUX and 1x4 DEMUX and validate outputs through FPGA implementation.
5. **Comparator Design (2-bit or 4-bit):** Design a simple digital comparator circuit that compares two binary inputs.
6. **Design and Implementation of a 4-bit Synchronous Counter:** To implement a 4-bit up/down synchronous counter using HDL, simulate for timing and logic correctness, and deploy it on FPGA hardware.
7. **Finite State Machine (FSM) Design:** Sequence Detector-To design a Moore or Mealy FSM for sequence detection, simulate the state transitions, and implement the design on an FPGA board.

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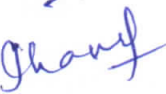
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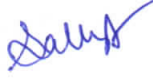
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8. **Design and Implementation of an ALU Supporting Basic Operations:** To design an Arithmetic Logic Unit that performs basic arithmetic and logic functions (ADD, SUB, AND, OR, NOT) and test it on FPGA.
9. **Interfacing Seven Segment Display with FPGA:** To write HDL code to drive a seven-segment display with binary or BCD inputs and implement the interface on FPGA hardware.
10. **Shift Register (Left/Right):** Design a shift register that shifts input bits left or right on each clock pulse.
11. **Implementation of Traffic Light Controller using FSM on FPGA:** To design a traffic light controller using finite state machines, simulate its time sequence, and implement it on FPGA hardware.
12. **PWM Signal Generation using FPGA:** To implement a pulse-width modulation (PWM) generator using Verilog HDL and demonstrate its use in applications like LED brightness control.
13. **Real-Time Clock Design and Display using FPGA:** To implement a real-time clock on FPGA with hour-minute-second display and use multiplexed seven-segment display for output.
14. **Serial Input with UART Receiver (Basic):** Implement a simple UART receiver to receive serial data and blink an LED.
15. **Implementing Digital Filters (FIR/IIR) on FPGA:** To implement a basic Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filter in HDL and simulate its output for given inputs.

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M.Tech. VLSI

L T P C

I Year – II Semester

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DISASTER MANAGEMENT

Course Objectives: Students will be able to

- learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches,
- planning and programming in different countries, particularly their home country or the countries they work in.

UNIT - I: Introduction

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India: Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT - II: Repercussions of Disasters and Hazards

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT - III: Disaster Preparedness and Management:

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

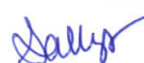
UNIT - IV: Risk Assessment Disaster Risk

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT - V: Disaster Mitigation:

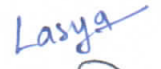
Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

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Text Books / Reference :

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies"
"New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.), "Disaster Mitigation Experiences and Reflections",
Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep
&Deep Publication Pvt. Ltd., New Delhi

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Vignan's Institute of Management and Technology for Women
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M.Tech.	L	T	P	C
II Year I Semester - VLSI System Design	3	0	0	3

CMOS RF IC Design

Course Overview

This course introduces the principles and design methodologies of CMOS Radio Frequency Integrated Circuits (RFICs). Students will learn to design and analyse critical RF building blocks such as low-noise amplifiers (LNAs), mixers, oscillators, and phase-locked loops (PLLs) in CMOS technology. Emphasis is placed on RF system-level understanding, noise and nonlinearity modeling, frequency planning, matching networks, and CMOS implementation strategies. The course combines theory, design practice, and simulation insights essential for modern wireless and communication IC design.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Analyse RF system-level parameters such as gain, noise figure, and non-linearity using standard performance metrics.
- Design CMOS small-signal amplifier circuits, including LNAs, with appropriate impedance matching and noise optimization techniques.
- Implement CMOS oscillator circuits such as LC and ring oscillators with attention to phase noise and frequency stability.
- Evaluate the performance of CMOS mixer circuits focusing on frequency conversion efficiency, linearity, and noise behaviour.
- Apply the principles of PLLs and frequency synthesizers to develop CMOS-based frequency generation solutions for RF systems.

Syllabus Unit I:

Introduction to RF Design and CMOS Technology: Review of RF system fundamentals - system gain, noise figure, nonlinearities, and link budget. Review of CMOS technology, basic MOSFET RF equivalent circuit model, advanced MOSFET RF equivalent circuit model, SPICE modeling of CMOS RF circuits – SPICE level 3 and BSIM parameters.

Unit II:

Small-Signal MOS Amplifier for RF: Basic amplifying structure, improvements to the basic amplifying structure, amplifier matching (LC and inductive), low-noise amplifiers (LNAs) – noise modeling for common source and common gate LNAs.

Unit III:

CMOS Oscillator Circuits: Review of general feedback principles, fixed-frequency oscillators, ring oscillator, voltage control of oscillators, oscillator phase noise and estimation.

Unit IV:

CMOS Mixer Circuits: General mixer concepts, single MOS mixer topologies, balanced MOSFET mixers, image rejection circuit topologies, I/Q mixer topologies.

Unit V:

CMOS PLLs and Frequency Synthesizers: Introduction to the phase lock loop – definitions and basic operation, phase detection and phase-frequency detection, loop filters, PLL noise behaviour, PLL behavioural modeling. Frequency Synthesis – PLL-based

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synthesizers, direct digital synthesis.

Text Book

1. Robert H. Caverly, *CMOS RFIC Design Principles*, Artech House, 2016.

Reference Books

1. Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 2nd Edition.
2. Behzad Razavi, *RF Microelectronics*, Prentice Hall, 2nd Edition.
3. R. Jacob Baker, *CMOS: Circuit Design, Layout, and Simulation*, Wiley IEEE Press, 3rd Edition.
4. Ali M. Niknejad, *RF CMOS: Modeling and Technology for Wireless Design*, Cambridge University Press.
5. David M. Pozar, *Microwave Engineering*, Wiley, 4th Edition.

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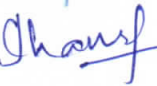
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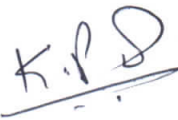
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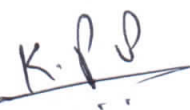
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Unit-V:

Hardware Security Primitives: Introduction, physical unclonable functions (PUFs), true random number generator (TRNG), design of anti-counterfeit, existing challenges and attacks. **Security and Trust Assessment:** Security assets and attack models, pre-silicon and post-silicon security and trust assessment.

Text Book

1. Bhunia, Swarup, and Mark M. Tehranipour. *Hardware Security: A Hands-on Learning Approach*. 1st ed., Academic Press, 2019.

Reference Books

1. Tehranipour, Mark, and Cliff Wang, editors. *Introduction to Hardware Security and Trust*. Springer, 2012.
2. Bhunia, Swarup, and Sandip Ray. *Fundamentals of IP and SoC Security: Design, Verification, and Debug*. Springer, 2017.
3. Wolf, Marilyn. *Embedded System Interfacing: Design for the Internet-of-Things (IoT)*. Morgan Kaufmann, 2019.
4. Skorobogatov, Sergei. *Semi-Invasive Attacks: A New Approach to Hardware Security Analysis*. Springer, 2007.

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Vignan's Institute of Management and Technology for Women
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M.Tech.	L	T	P	C
II Year I Semester - VLSI System Design	3	0	0	3

Advanced Memory Design and Architectures

Course Overview

This course provides an in-depth exploration of memory systems and architectures in modern and next-generation computer systems. Starting from the foundational concepts of caching and memory hierarchy, the course advances through on-chip network design, multicore memory consistency, DRAM system architectures, and emerging non-volatile memory technologies. It emphasizes architectural modeling, performance optimization, and system-level design trade-offs relevant to current and future computing platforms, including those used in high-performance and embedded systems.

Course Outcomes (COs)

By the end of this course, students will be able to:

- Describe the structure, operation, and performance aspects of cache memory systems, including advanced designs like trace caches and prefetching.
- Analyse the architecture and performance of on-chip networks (NoCs), including routing mechanisms and router design.
- Explain memory models, identify data races, and apply concepts like transactional memory in multicore systems.
- Illustrate the organization and timing of DRAM systems and evaluate the role of memory controllers.
- Compare various emerging memory technologies and recommend suitable types for specific system-level applications

Syllabus Unit I:

Caches: Memory hierarchy and the notion of caches, virtual memory, modeling and designing a cache, advanced cache design, trace caches, instruction prefetching, data prefetching.

Unit II:

The On-chip Network: Overview of an NoC, message transmission, routing, design of a router, non-uniform cache architectures, performance aspects.

Unit III:

Multicore Systems: Parallel programming, issues in parallel hardware, theoretical foundations of memory models, memory models, data races, transactional memory.

Unit IV:

DRAMs: DRAM cell, capacitors used in DRAM cells, array of DRAM cells, a computer system with DRAM arrays, design spaces of DRAMs, DDR generations and timing, buffered DIMMs, DRAM access protocols, DRAM timing, memory controller.

Unit V:

Emerging Memory Technologies: Flash memory, ferroelectric RAM (FeRAM), magnetoresistive RAM (MRAM), phase change memory (PCM), resistive RAM (ReRAM), 3D and embedded memory technologies.

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Unit-IV:

Carbon Nanotubes (CNTs): Introduction to CNTs, Synthesis of CNTs (arc-discharge, laser- ablation, catalytic growth), Growth mechanisms of CNTs, Multi-walled nanotubes, Single-walled nanotubes, Optical properties of CNTs, Electrical transport in perfect nanotubes, Applications of CNTs.

Unit-V:

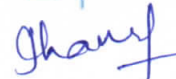
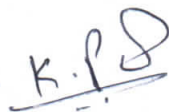
Advanced Nanomaterials and Applications: Ferroelectric materials, Coating, Molecular electronics, Nanoelectronics, Biological and environmental applications, Membrane-based applications, Polymer-based applications.

Text Book

1. I. Gusev and A. A. Rempel. *Nanocrystalline Materials*. Cambridge International Science Publishing; 1st Indian edition, Viva Books Pvt. Ltd., 2008.
2. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, and James Murday. *Nanoscience and Nanotechnology*. Tata McGraw-Hill Education, 2012.

Reference Books

1. Kenneth J. Klabunde and Ryan M. Richards, editors. *Nanoscale Materials in Chemistry*. 2nd ed., John Wiley & Sons, 2009.
2. Bharat Bhushan. *Springer Handbook of Nanotechnology*. 3rd ed., Springer, 2010.
3. Kamal K. Kar. *Carbon Nanotubes: Synthesis, Characterization and Applications*. 1st ed., Research Publishing Services, 2011.

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BUSINESS ANALYTICS

Course Objectives:

- Understand the role of business analytics within an organization. Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization.
- To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making.
- To become familiar with processes needed to develop, report, and analyze business data.
- Use decision-making tools/Operations research techniques.
- Manage business process using analytical and management tools.
- Analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospace etc.

Course Outcomes: Students will demonstrate knowledge of data analytics.

- Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.
- Students will demonstrate the ability to use technical skills in predicative and prescriptive modelling to support business decision-making.
- Students will demonstrate the ability to translate data into clear, actionable insights.

UNIT - I: Business analytics

Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.

UNIT - II: Trendiness and Regression Analysis:

Modelling Relationships and Trends in Data, simple Linear Regression, Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

UNIT - III :

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

UNIT - IV: Forecasting Techniques

Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models

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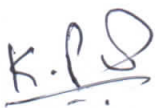
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for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carlo Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT - V: Decision Analysis

Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making. Recent Trends in Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

Text Books:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

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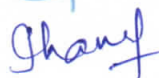
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INDUSTRIAL SAFETY

Course Objectives:

- To provide information regarding different elements of industrial water pollution and Methods of treatment.
- To expose to the various industrial applications, maintenance, preventive measures taken against wear and tear.

Course Outcomes: At the end of the course, student will be able to:

- Know how to take safety measures in executing works
- Identify the need for maintenance (or) replacement of equipment
- Understand the need for periodic and preventive maintenance.

UNIT - I: Industrial safety

Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT - II: Fundamentals of maintenance engineering:

Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT - III : Wear and Corrosion and their prevention

Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications,

- i. Screw down grease cup,
- ii. Pressure grease gun,
- iii. Splash lubrication,
- iv. Gravity lubrication,
- v. Wick feed lubrication
- vi. Side feed lubrication,
- vii. Ring lubrication,

Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods

UNIT - IV Fault tracing:

Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault-finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like,

- i. Any one machine tool,
- ii. Pump
- iii. Air compressor
- iv. Internal combustion engine,

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Unit-V:

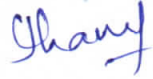
Machine Learning in Physical Design: Introduction ML promises and challenges in physical design, Canonical ML applications, the state of ML for physical design.

Text Book

1. Kahng, Andrew B., et al. *VLSI Physical Design: From Graph Partitioning to Timing Closure*. 2nd ed., Springer International Publishing, 2022.
2. Sherwani, Naveed A. *Algorithms for VLSI Physical Design Automation*. 3rd ed., Springer, 2012.

Reference Books

1. Hsiao, Michael. *Machine Learning Applications in Electronic Design Automation*. Morgan & Claypool, 2020.
2. Cong, Jason, and Bei Yu. *Machine Learning and AI for EDA: From Fundamentals to Advanced Applications*. Springer, 2022.

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Operations Research

Course Outcomes: At the end of the course, the student should be able to

- Students should be able to apply the dynamic programming to solve problems of discrete and continuous variables.
- Students should be able to apply the concept of non-linear programming
- Students should be able to carry out sensitivity analysis
- Student should be able to model the real-world problem and simulate it.

UNIT - I:

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

UNIT - II:

Formulation of a LPP - Graphical solution revised simplex method - duality theory – dual simplex method - sensitivity analysis - parametric programming

UNIT - III :

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem – max flow problem - CPM/PERT

UNIT – IV:

Scheduling and sequencing - single server and multiple server models – deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT - V:

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

Text Books /References:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008.
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, Delhi, 2008.
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009.
5. Pannerselvam, Operations Research: Prentice Hall of India 2010.
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010.

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M.Tech. VLSI**L T P C****II Year – I Semester****3 0 0 3**

COST MANAGEMENT OF ENGINEERING PROJECTS

UNIT – I:

Introduction and Overview of the Strategic Cost Management Process Cost concepts in decision making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

UNIT - II:

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre-project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

UNIT - III:

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints.

UNIT – IV:

Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

UNIT - V:

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

Text Books/References:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Lt

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COMPOSITE MATERIALS

UNIT - I:INTRODUCTION

Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT – II:REINFORCEMENTS

Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions

UNIT - III :Manufacturing of Metal Matrix Composites

Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT – IV:Manufacturing of Polymer Matrix Composites

Preparation of Moulding compounds and preregs –hand layup method – Autoclave method – Filament winding method – Compression moulding –Reaction injection moulding. Properties and applications.

UNIT - V: Strength

Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first ply failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

Text Books/References:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R.Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.
3. Hand Book of Composite Materials-ed-Lubin.
4. Composite Materials – K. K. Chawla.
5. Composite Materials Science and Applications – Deborah D. L. Chung.
6. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi

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