JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING
COURSE STRUCTURE & SYLLABUS (R18)

Applicable From 2018-19 Admitted Batch

I YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	MA101BS	Mathematics - I	3	1	0	4
2	AP102BS	Applied Physics	3	1	0	4
3	CS103ES	Programming for Problem Solving	3	1	0	4
4	ME104ES	Engineering Graphics	1	0	4	3
5	AP105BS	Applied Physics Lab	0	0	3	1.5
6	CS106ES	Programming for Problem Solving Lab	0	0	3	1.5
7	*MC109ES	Environmental Science	3	0	0	0
		Induction Programme				
		Total Credits	**13**	**3**	**10**	**18**

I YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	MA201BS	Mathematics - II	3	1	0	4
2	CH202BS	Chemistry	3	1	0	4
3	EE203ES	Basic Electrical Engineering	3	0	0	3
4	ME205ES	Engineering Workshop	1	0	3	2.5
5	EN205HS	English	2	0	0	2
6	CH206BS	Engineering Chemistry Lab	0	0	3	1.5
7	EN207HS	English Language and Communication Skills Lab	0	0	2	1
8	EE208ES	Basic Electrical Engineering Lab	0	0	2	1
		Total Credits	**12**	**2**	**10**	**19**

II YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC301PC	Electronic Devices and Circuits	3	1	0	4
2	EC302PC	Network Analysis and Transmission Lines	3	0	0	3
3	EC303PC	Digital System Design	3	1	0	4
4	EC304PC	Signals and Systems	3	1	0	4
5	EC305ES	Probability Theory and Stochastic Processes	3	0	0	3
6	EC306PC	Electronic Devices and Circuits Lab	0	0	2	1
7	EC307PC	Digital System Design Lab	0	0	2	1
8	EC308ES	Basic Simulation Lab	0	0	2	1
9	*MC309	Constitution of India	3	0	0	0
		Total Credits	**18**	**3**	**6**	**21**

II YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	MA401BS	Laplace Transforms, Numerical Methods & Complex Variables	3	1	0	4
2	EC402PC	Electromagnetic Fields and Waves	3	0	0	3

3	EC403PC	Analog and Digital Communications	3	1	0	4
4	EC404PC	Linear IC Applications	3	0	0	3
5	EC405PC	Electronic Circuit Analysis	3	0	0	3
6	EC406PC	Analog and Digital Communications Lab	0	0	3	1.5
7	EC407PC	IC Applications Lab	0	0	3	1.5
8	EC408PC	Electronic Circuit Analysis Lab	0	0	2	1
9	*MC409	Gender Sensitization Lab	0	0	2	0
		Total Credits	**15**	**2**	**10**	**21**

III YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC501PC	Microprocessors & Microcontrollers	3	1	0	4
2	EC502PC	Data Communications and Networks	3	1	0	4
3	EC503PC	Control Systems	3	1	0	4
4	SM504MS	Business Economics & Financial Analysis	3	0	0	3
5		Professional Elective - I	3	0	0	3
6	EC505PC	Microprocessors & Microcontrollers Lab	0	0	3	1.5
7	EC506PC	Data Communications and Networks Lab	0	0	3	1.5
8	EN508HS	Advanced Communication Skills Lab	0	0	2	1
9	*MC510	Intellectual Property Rights	3	0	0	0
		Total Credits	**18**	**3**	**8**	**22**

III YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC601PC	Antennas and Propagation	3	1	0	4
2	EC602PC	Digital Signal Processing	3	1	0	4
3	EC603PC	VLSI Design	3	1	0	4
4		Professional Elective - II	3	0	0	3
5		Open Elective - I	3	0	0	3
6	EC604PC	Digital Signal Processing Lab	0	0	3	1.5
7	EC605PC	e – CAD Lab	0	0	3	1.5
8	EC606PC	Scripting Languages Lab	0	0	2	1
9	*MC609	Environmental Science	3	0	0	0
		Total Credits	**18**	**3**	**8**	**22**

IV YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC701PC	Microwave and Optical Communications	3	0	0	3
2		Professional Elective – III	3	0	0	3
3		Professional Elective – IV	3	0	0	3
4		Open Elective - II	3	0	0	3
5	SM702MS	Professional Practice, Law & Ethics	2	0	0	2
6	EC703PC	Microwave and Optical Communications Lab	0	0	2	1
7	EC704PC	Industrial Oriented Mini Project/ Summer Internship	0	0	0	2*
8	EC705PC	Seminar	0	0	2	1
9	EC706PC	Project Stage - I	0	0	6	3
		Total Credits	**14**	**0**	**10**	**21**

IV YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1		Professional Elective – V	3	0	0	3
2		Professional Elective – VI	3	0	0	3
3		Open Elective - III	3	0	0	3
4	EC801PC	Project Stage - II	0	0	14	7
		Total Credits	**9**	**0**	**14**	**16**

***MC - Environmental Science – Should be Registered by Lateral Entry Students Only.**
***MC – Satisfactory/Unsatisfactory**

Note: Industrial Oriented Mini Project/ Summer Internship is to be carried out during the summer vacation between 6th and 7th semesters. Students should submit report of Industrial Oriented Mini Project/ Summer Internship for evaluation.

Professional Elective – I

EC511PE	Computer Organization & Operating Systems
EC512PE	Error Correcting Codes
EC513PE	Electronic Measurements and Instrumentation

Professional Elective – II

EC611PE	Object Oriented Programming through Java
EC612PE	Mobile Communications and Networks
EC613PE	Embedded System Design

Professional Elective – III

EC711PE	Artificial Neural Networks
EC712PE	Scripting Languages
EC713PE	Digital Image Processing

Professional Elective – IV

EC721PE	Biomedical Instrumentation
EC722PE	Database Management Systems
EC723PE	Network Security and Cryptography

Professional Elective – V

EC811PE	Satellite Communications
EC812PE	Radar Systems
EC813PE	Wireless Sensor Networks

Professional Elective – VI

EC821PE	System on Chip Architecture
EC822PE	Test and Testability
EC823PE	Low Power VLSI Design

EC811PE : SATELLITE COMMUNICATIONS (PE – V)

B.Tech. IV Year II Semester

L	T	P	C
3	0	0	3

Prerequisite: Analog and Digital Communications

Course Objectives :

- To acquired foundation in orbital mechanics and launch vehicles for the satellites.
- To provide basic knowledge of link design of satellite.
- To understand multiple access systems and earth station technology
- To understand the concepts of satellite navigation and GPS.

Course Outcomes: Upon completing this course, the student will be able to

- Understand basic concepts and frequency allocations for satellite communication, orbital mechanics and launch vehicles.
- Envision the satellite sub systems and design satellite links for specified C/N.
- Understand the various multiple access techniques for satellite communication systems and earth station technologies.
- Known the concepts of LEO, GEO Stationary Satellite Systems and satellite navigation

UNIT - I:

Introduction: Origin of Satellite Communications, Historical Back-ground, Basic Concepts of Satellite Communications, Frequency Allocations for Satellite Services, Applications, Future Trends of Satellite Communications.

Orbital Mechanics and Launchers: Orbital Mechanics, Look Angle determination, Orbital Perturbations, Orbit determination, Launches and Launch vehicles, Orbital Effects in Communication Systems Performance.

UNIT - II:

Satellite Subsystems: Attitude and Orbit Control System, Telemetry, Tracking, Command And Monitoring, Power Systems, Communication Subsystems, Satellite Antennas, Equipment Reliability and Space Qualification.

UNIT - III:

Satellite Link Design: Basic Transmission Theory, System Noise Temperature and G/T Ratio, Design of Down Links, Up Link Design, Design Of Satellite Links For Specified C/N, System Design Examples.

Multiple Access: Frequency Division Multiple Access (FDMA), Inter modulation, Calculation of C/N, Time Division Multiple Access (TDMA), Frame Structure, Examples, Satellite Switched TDMA Onboard Processing, DAMA, Code Division Multiple Access (CDMA), Spread Spectrum Transmission and Reception.

UNIT - IV:

Earth Station Technology: Introduction, Transmitters, Receivers, Antennas, Tracking Systems, Terrestrial Interface, Primary Power Test Methods.

UNIT - V:

Low Earth Orbit and Geo-Stationary Satellite Systems: Orbit Considerations, Coverage and Frequency Consideration, Delay & Throughput Considerations, System Considerations, Operational NGSO Constellation Designs.

Satellite Navigation & Global Positioning System: Radio and Satellite Navigation, GPS Position Location Principles, GPS Receivers and Codes, Satellite Signal Acquisition, GPS Navigation Message, GPS Signal Levels, GPS Receiver Operation, GPS C/A Code Accuracy, Differential GPS.

TEXT BOOKS:

1. Satellite Communications – Timothy Pratt, Charles Bostian and Jeremy Allnutt, WSE, Wiley Publications, 2nd Edition, 2003.

2. Satellite Communications Engineering – Wilbur L. Pritchard, Robert A Nelson and Henri G. Suyderhoud, 2nd Edition, Pearson Publications, 2003.

REFERENCE BOOKS:

1. Satellite Communications : Design Principles – M. Richharia, BS Publications, 2nd Edition, 2003.
2. Satellite Communication - D.C Agarwal, Khanna Publications, 5th Ed.
3. Fundamentals of Satellite Communications – K.N. Raja Rao, PHI, 2004
4. Satellite Communications – Dennis Roddy, McGraw Hill, 4th Edition, 2009.

EC812PE: RADAR SYSTEMS (PE – V)

B.Tech. IV Year II Semester

L	T	P	C
3	0	0	3

Prerequisite: Analog and Digital Communications

Course Objectives:

- To explore the concepts of radar and its frequency bands.
- To understand Doppler effect and get acquainted with the working principles of CW radar, FM-CW radar.
- To impart the knowledge of functioning of MTI and Tracking Radars.
- To explain the deigning of a Matched Filter in radar receivers.

Course Outcomes: Upon completing this course, the student will be able to

- Derive the complete radar range equation.
- Understand the need and functioning of CW, FM-CW and MTI radars
- Known various Tracking methods.
- Derive the matched filter response characteristics for radar receivers.

UNIT - I

Basics of Radar: Maximum Unambiguous Range, Simple form of Radar Equation, Radar Block Diagram and Operation, Radar Frequencies and Applications. Prediction of Range Performance, Minimum Detectable Signal, Receiver Noise, Modified Radar Range Equation.

Radar Equation: SNR, Envelope Detector – False Alarm Time and Probability, Integration of Radar Pulses, Radar Cross Section of Targets, Transmitter Power, PRF and Range Ambiguities, System Losses (qualitative treatment).

UNIT - II

CW and Frequency Modulated Radar: Doppler Effect, CW Radar – Block Diagram, Isolation between Transmitter and Receiver, Non-zero IF Receiver, Receiver Bandwidth Requirements, Applications of CW radar.

FM-CW Radar: Range and Doppler Measurement, Block Diagram and Characteristics, FM-CW altimeter.

UNIT - III

MTI and Pulse Doppler Radar: Principle, MTI Radar - Power Amplifier Transmitter and Power Oscillator Transmitter, Delay Line Cancellers – Filter Characteristics, Blind Speeds, Double Cancellation, Staggered PRFs. Range Gated Doppler Filters. MTI Radar Parameters, Limitations to MTI Performance, MTI versus Pulse Doppler Radar.

UNIT - IV

Tracking Radar: Tracking with Radar, Sequential Lobing, Conical Scan, Mono pulse Tracking Radar – Amplitude Comparison Mono pulse (one- and two- coordinates), Phase Comparison Mono pulse, Tracking in Range, Acquisition and Scanning Patterns, Comparison of Trackers.

UNIT - V

Detection of Radar Signals in Noise Matched Filter Receiver – Response Characteristics and Derivation, Correlation Function and Cross-correlation Receiver, Efficiency of Non-matched Filters, Matched Filter with Non-white Noise.

Radar Receivers – Noise Figure and Noise Temperature, Displays – types. Duplexers – Branch type and Balanced type, Circulators as Duplexers. Introduction to Phased Array Antennas – Basic Concepts, Radiation Pattern, Beam Steering and Beam Width changes, Applications, Advantages and Limitations.

TEXT BOOKS:

1. Introduction to Radar Systems – Merrill I. Skolnik, TMH Special Indian Edition, 2nd Ed., 2007.

REFERENCE BOOKS:

1. Radar: Principles, Technology, Applications – Byron Edde, Pearson Education, 2004.

2. Radar Principles – Peebles, Jr., P.Z., Wiley, New York, 1998.
3. Principles of Modern Radar: Basic Principles – Mark A. Richards, James A. Scheer, William A. Holm, Yesdee, 2013
4. Radar Handbook - Merrill I. Skolnik, 3rd Ed., McGraw Hill Education, 2008.

EC813PE: WIRELESS SENSOR NETWORKS (PE – V)

B.Tech. IV Year II Semester

L	T	P	C
3	0	0	3

Prerequisite: Analogue and Digital Communications

Course Objectives:

- To acquire the knowledge about various architectures and applications of Sensor Networks
- To understand issues, challenges and emerging technologies for wireless sensor networks
- To learn about various routing protocols and MAC Protocols
- To understand various data gathering and data dissemination methods
- To Study about design principals, node architectures, hardware and software required for implementation of wireless sensor networks.

Course Outcomes: Upon completion of the course, the student will be able to:

- Analyze and compare various architectures of Wireless Sensor Networks
- Understand Design issues and challenges in wireless sensor networks
- Analyze and compare various data gathering and data dissemination methods.
- Design, Simulate and Compare the performance of various routing and MAC protocol

UNIT - I:
Introduction to Sensor Networks, unique constraints and challenges, Advantage of Sensor Networks, Applications of Sensor Networks, Types of wireless sensor networks

UNIT - II:
Mobile Ad-hoc Networks (MANETs) and Wireless Sensor Networks, Enabling technologies for Wireless Sensor Networks. Issues and challenges in wireless sensor networks

UNIT - III:
Routing protocols, MAC protocols: Classification of MAC Protocols, S-MAC Protocol, B-MAC protocol, IEEE 802.15.4 standard and ZigBee

UNIT - IV:
Dissemination protocol for large sensor network. Data dissemination, data gathering, and data fusion; Quality of a sensor network; Real-time traffic support and security protocols.

UNIT - V:
Design Principles for WSNs, Gateway Concepts Need for gateway, WSN to Internet Communication, and Internet to WSN Communication.
Single-node architecture, Hardware components & design constraints,
Operating systems and execution environments, introduction to TinyOS and nesC.

TEXT BOOKS:

1. Ad-Hoc Wireless Sensor Networks- C. Siva Ram Murthy,B. S. Manoj, Pearson
2. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE

REFERENCE BOOKS:

1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.
4. Wireless Communication and Networking – William Stallings, 2003, PHI.

EC821PE: SYSTEM ON CHIP ARCHITECTURE (PE – VI)

B.Tech. IV Year II Semester

L	T	P	C
3	0	0	3

Prerequisite: Embedded System Design

Course Objectives:
- To introduce the architectural features of system on chip.
- To imbibe the knowledge of customization using case studies.

Course Outcomes:
- Expected to understand SOC Architectural features.
- To acquire the knowledge on processor selection criteria and limitations
- To acquires the knowledge of memory architectures on SOC.
- To understands the interconnection strategies and their customization on SOC.

UNIT – I:
Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II:
Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III:
Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I , and D – Caches , Multilevel Caches, Virtual to real translation , SOC Memory System , Models of Simple Processor – memory interaction.

UNIT - IV:
Interconnect Customization: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization:

UNIT – V:
Configuration: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

TEXT BOOKS:
1. Computer System Design System-on-Chip by Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Eed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:
1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

EC822PE: TEST AND TESTABILITY (PE – VI)

B.Tech. IV Year II Semester

L	T	P	C
3	0	0	3

Prerequisite: Switching Theory and Logic Design, Digital System Design with PLDS

Course Objectives:
- To provide or broad understanding of fault diagnosis.
- To illustrate the framework of test pattern generation.
- To understand design for testability in Digital Design

Course Outcomes: On completion of this course the student will be able to:
- To acquire the knowledge of fundamental concepts in fault and fault diagnosis
- Test pattern generation using LFSR and CA
- Design for testability rules and techniques for combinational circuits
- Introducing scan architectures

UNIT - I
Need for testing, the problems in digital Design testing, the problems in Analog Design testing, the problems in mixed analog/digital design testing, design for test, printed-circuit board (PCB) testing, software testing,
Fault in Digital Circuits:
General Introduction, Controllability and Observability, Fault Models, stuck at faults, bridging faults, CMOS technology considerations, intermittent faults.

UNIT - II
General Introduction, to test pattern genration, Test Pattern generation for combinational logic circuits, Manual test pattern generation, automatic test pattern generation, boolen difference method, Roth's D-algoritham, Developments following Roth's D-algoritham, Pseudorandom test pattern generation.

UNIT - III
Pseudorandorn test pattern generators, Design of test pattern generator usingLinear feedback shift registers (LFSRs) and cellular automata(CAs).

UNIT - IV
Design for Testability for combinational circuits: Basic Concepts of testability, controllability and observability, the Reed Muller's expansion techniques, use of control logic and syndrome testable designs.

UNIT - V
Making sequential circuits testable, testability insertion, full scan DFT technique-Full scan insertion, flip-flop structures, Full scan design and test, scan architectures-full scan design, shadow register DFT, partial scan methods, multiple scan design, other scan designs.

TEXT BOOKS
1. Fault Tolerant and Fault Testable Hardware Design-Parag K. Lala, 1984, PHI.
2. VLSI Testing digital and Mixed analogue/digital techniques-Stanley L. Hurst, IEE Circuits, Devices and Systems series 9, 1998.

REFERENCE BOOKS
1. Digital Systems Testing and Testable Design-Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, Jaico Books
2. Esstentials of Electronic Testing-Bushnell and Vishwani D.Agarwal, Springers.
3. Design for test for Digital IC's and Embedded Core Systems-Alfred L. Crouch, 2008, Pearson Education.

EC823PE: LOW POWER VLSI DESIGN (PE – VI)

B.Tech. IV Year II Semester

L	T	P	C
3	0	0	3

Prerequisite: VLSI Design

Course Objectives:

- Known the low power low voltage VLSI design
- Understand the impact of power on system performances.
- Known about different Design approaches.
- Identify suitable techniques to reduce power dissipation in combinational and sequential circuits.

Course Outcomes: Upon completing this course, the student will be able to

- Understand the need of Low power circuit design.
- Attain the knowledge of architectural approaches.
- Analyze and design Low-Voltage Low-Power combinational circuits.
- Known the design of Low-Voltage Low-Power Memories

UNIT - I:

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT - II:

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, and Mask level Measures.

UNIT - III:

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT - IV:

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT - V:

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
3. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
4. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, Anatha Chandrakasan, Springer, 2005.